NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

PRACTICAL IMPLEMENTATION OF THE HARD SWITCHED BUCK CHOPPER

by

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March 1997

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REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE March 1997.	3. REPORT TYPE AND DATES COVERED Master's Thesis

4. TITLE AND SUBTITLE TITLE OF THESIS. PRACTICAL IMPLEMENTATION OF THE HARD SWITCHED BUCK CHOPPER

5. FUNDING NUMBERS

6. AUTHOR(S) Kirk D. Allen

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

As the Navy progresses into the twenty-first century, new concepts in shipboard electrical power management are being explored. One area of significant interest to the Navy is utilization of DC electrical distribution systems rather than traditional AC distribution systems. The DC Zonal Electrical Distribution System is a prime candidate for direct application to modern power distribution. This system employs solid-state conversion devices to supply ships loads from one of two high-voltage DC busses. One such device, a buck chopper, is the focus of this thesis. In order to validate this proposed architecture, the startup and transient performance of these choppers must be explored. The buck chopper incorporates a control technique which employs both voltage and current feedback in conjunction with feed-forward. Specific advantages of this control technique with the buck chopper circuit include power source perturbation rejection, fast dynamic response to both load and source voltage changes and a house curve for parallel buck chopper operation. The design will include both over-current and thermal protection in order to prevent circuit component damage. The focus of this thesis is to validate the predicted operation of this control technique and to verify circuit performance.

14. SUBJECT TERMS Closed Loop Feedback with Feed Forward Control, PEBB, Buck Converter, Matlab, Simulink.

15. NUMBER OF PAGES 129

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18 298-102

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PRACTICAL IMPLEMENTATION OF THE HARD SWITCHED BUCK CHOPPER

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 1997

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ABSTRACT

As the Navy progresses into the twenty-first century, new concepts in shipboard electrical power management are being explored. One area of significant interest to the Navy is utilization of DC electrical distribution systems rather than traditional AC distribution systems. The DC Zonal Electrical Distribution System is a prime candidate for direct application to modern power distribution. This system employs solid-state conversion devices to supply ships loads from one of two high-voltage DC busses. One such device, a buck chopper, is the focus of this thesis. In order to validate this proposed architecture, the startup and transient performance of these choppers must be explored. The buck chopper incorporates a control technique which employs both voltage and current feedback in conjunction with feed-forward. Specific advantages of this control technique with the buck chopper circuit include power source perturbation rejection, fast dynamic response to both load and source voltage changes and a house curve for parallel buck chopper operation. The design will include both over-current and thermal protection in order to prevent circuit component damage. The focus of this thesis is to validate the predicted operation of this control technique and to verify circuit performance.

TABLE OF CONTENTS

I. INTRODUCTION 1

A. RESEARCH FOCUS 1

B. DC ZONAL ELECTRICAL DISTRIBUTION SYSTEM 2

II. THE POWER SECTION 7

A. GENERAL DESCRIPTION 7

1. Basic Buck Chopper Topology 7

2. Component Selection 12

B. IGBT DRIVER CIRCUIT 15

C. POWER SECTION TEST RESULTS 17

D. CORE SIZING 18

E. PHYSICAL LAYOUT 24

III. CLOSED-LOOP FEEDBACK WITH FEED-FORWARD 29

A. BASIS FOR OPERATION 29

1. Theory of Operation 29

2. State-Space Representation 35

3. Feed-Forward Control 37

4. Integrator-Based Feedback 38

5. Multiloop 39

6. State Difference 40

B. PROTECTIVE FEATURES 44

IV. COMPUTER SIMULATION 47

A. OVERVIEW 47

B. CONTROLLER MODEL 50

1. Buck Chopper Startup 50

2. Source Voltage Sinusoidal Variation 52

3. Step Change In Source Voltage 54

4. Source Voltage Droop 57

5. Load Transcent Analysis 58

C. PARALLEL OPERATIONS 62

1. Startup of a Second Choper 61

2. Dynamic Load Environment 64

V. PROTOTYPE CONTROLLER 67

A. CONTROL CIRCUIT DESIGN 67

1. Power Supplies 69

2. 25 Pin Connector and Buffer Stage 70

3. Main Control Stage 71
4. PWM Circuit 74
5. Protection, Startup and Reference Stage 75

B. SENSOR BOARD CIRCUIT DESIGN 78
1. Power Supply Circuit 79
2. Voltage Measuring Circuit 79
3. Current Sensing Circuit 80

C. PHASE-LOCKED LOOP 81

D. CONTROLLER BENCH TESTS 82
1. Output Waveform Verification 83
2. Pulse-By-Pulse Over-Current Protection 84
3. Time Out Over-Current Protection 85

E. SINGLE BUCK CHOPPER OPERATION WITH FEEDBACK 85
1. Buck Chopper Startup and Ripple Rejection 86
2. Source Voltage Droop 87
3. Load Regulation 88

F. PARALLEL OPERATIONS 90
1. Buck Chopper Startup 91
2. Load Regulation 93

VI. CONCLUSIONS AND RECOMMENDATIONS 95

A. SUMMARY OF RESULTS 95

B. FUTURE RESEARCH AREAS 98
1. Digital Signal Processing Application 98

LIST OF REFERENCES 99

APPENDIX A. IGBT DATA SHEETS 101

APPENDIX B. MATLAB FEEDBACK GAIN CODE 109

APPENDIX C NETLIST CONTROLLER,PLL AND IGBT DRIVER CIRCUIT 119

INITIAL DISTRIBUTION LIST 129

I. INTRODUCTION

A. RESEARCH FOCUS

The purpose of this thesis research is to define and document the operating and startup procedures for the hard-switched DC-to-DC buck choppers being utilized in the Power Electronic Building Block(PEBB) testbed. The PEBB testbed serves as an analysis tool for studying a prototype portion of future Naval power distribution systems. The buck choppers consist of a power section and a controller that implements closed-loop feedback with feed-forward.

As the Navy searches for new and better ways to improve the performance, reliability, and simplicity of modern warships, basic research into concepts facilitating this goal must be undertaken. In the arena of power distribution systems, a future design has been suggested by Dade [7] in which the primary power transmission lines of the vessel would carry DC power at fairly high voltage levels. The power from these busses would be distributed throughout the vessel by the use of solid-state power conversion devices. The devices must be able to convert the distributed DC voltage level to the DC or AC voltage levels of the loads. A modular control system which is able to perform these functions reliably and simply would be of great benefit to future ship power system designers. Integral to this proposed architecture is the proper operation of the DC-to-DC buck chopper. Effective control will allow for utilization in these future power systems due to the inherent simplicity of the control technique and the possibility of modular

design. This research will document the startup and operating procedures for the hard-switched buck chopper.

The areas explored include a theoretical development of closed-loop control and simulations of a single buck chopper for startup, load changes and overload conditions. Also to be explored is the parallel operation of buck choppers into a load to determine those individual specifications that must be guaranteed to prevent circuit degradation. A description of the DC-to-DC buck chopper, including driver circuit, power conditioning, inductor core sizing, and buck chopper physical layout is included in Chapter II. In Chapter III, the theoretical basis for closed loop feed-forward control is presented. The simulation results of the basic controller, and open and closed-loop control of the buck chopper are reported in Chapter IV. In Chapter V, the prototype controller topology and performance characteristics of the basic controller, open-loop control, and closed-loop control bench tests are documented. The conclusions of this research and recommended future studies are described in Chapter VI.

B. DC ZONAL ELECTRICAL DISTRIBUTION SYSTEM

One particularly interesting shipboard electrical distribution system, advocated and described by Doerry [6], is the DC Zonal Electrical Distribution System (DC ZEDS). This system promotes modularity of design within vessels by specifying that there be only main power generation equipment, a port and starboard main power DC bus and all other electrical distribution achieved through the use of DC zones. Figure (1-1) illustrates the basic topology of a zone within the DC ZEDS architecture. The port and starboard

DC busses for each zone carry 1000 V DC power throughout the ship with higher voltages possible as semiconductor switch capabilities improve. A Ship Service Converter Module (SSCM) receives the 1000V DC input and produces a regulated power at a lower DC voltage for use in Ship Service Inverter Modules (SSIM) and intermediate voltage DC loads. The SSIM takes the lower DC voltage from the SSCM and converts it into regulated AC power for use in the ships AC loads. Vital loads would utilize both main power busses through diode steering.

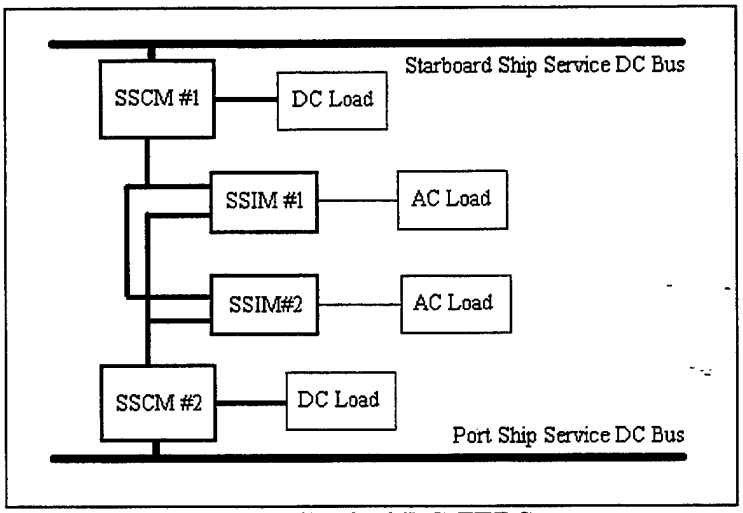


Figure 1-1, Typical DC ZEDS zone

The voltage ratings of the SSCMs depend on where in the zone the unit is located and, of course, power ratings are dictated by the attached load. The AC outputs of the SSIMs would be at various voltage levels and frequencies in order to supply all different types of AC loads.

Some advantages of utilizing a zonal DC power distribution system with dispersed solid-state power converters are cost savings associated with the elimination of

large electromechanical switchgear, optimization of the power generation equipment to provide only the main DC power busses, minimization of power conversion steps between generator and end user, and the potential advantage of fast semiconductor devices improving shipboard power management under normal and casualty conditions. Also of great interest is the commonality and modularity of the major building blocks within the DC ZEDS concept. The Navy could save appreciably in the reduced training and manning requirements as the electrical power distribution systems across the classes of ships become more common. In addition, as future technologies come to fruition, the best power conversion modules available can be easily implemented into the system by ensuring interface criteria are met.

One such technology discussed by Doerry is the Power Electronic Building Block [6]...

"The Power Electronic Building Block (PEBB) is a new device that integrates within a single unit, all the elements required for generalized power processing. It will replace many single application multi-component power control circuits with a single device that delivers digitally synthesized power under device level control. PEBBs are a standard set of snap together parts that start at the semiconductor chip level and build up to the system level while integrating intelligence at various levels for custom performance - a power electronic analogy of a microprocessor. Clearly this is an exciting possibility for the future of power electronics; however, copious amounts of basic research must be accomplished before such a device can be realized."

For now, the SSCM and SSIM must take on the roles as the major power conversion devices within the DC ZEDS architecture. The SSCM must necessarily be a DC step-down converter. One of the most popular topologies for this conversion process is the buck chopper, whose operating and startup procedures must be thoroughly explored. This topology was originally outlined by Morgan[13] for large power applications utilizing solid state switches. The SSIM could be one of many inverter topologies; however, the basic control needs for these topologies will be realized using Digital Signal Processing and near real-time control. Utilizing this approach, the exact control scheme could be changed with little if any modifications required to the existing hardware. The selected control technique must be extendible to any type of switching control scenario encountered by the types of converters described.

The buck chopper will be initially analyzed open loop to determine switching losses, inductor performance and output voltage ripple. Closed-loop testing will include transient testing for startup with load. This testing will validate the design parameters of the controller. Transient load testing of a single buck chopper will be analyzed for correct controller, suitable transient output voltage response and verification of the house curve, which is necessary for load sharing. The last portion of testing will be the transient load analysis of two buck choppers operating in parallel.

The testbed developed for the closed-loop feed-forward controller incorporates a buck chopper. This will allow for testing the capabilities of the technique in an application which is fundamental to the DC ZEDS architecture. A basic derivation of the governing equations for a buck chopper is presented in the next chapter, along with a

description of the physical testbed built for the prototype controller. Chapter III will outline the basis for the governing control equation and discuss circuit protective features incorporated in the controller. Chapter IV will explore the computer simulation of the buck chopper and controller model for startup, load regulation, source perturbation rejection and parallel operations. Chapter V will discuss the prototype controller utilized for this research. Finally, Chapter VI will summarize the results and explore future research areas.

II. THE POWER SECTION

A. GENERAL DESCRIPTION

The buck chopper, or step-down converter, is a DC-to-DC converter in which the input voltage is cyclically switched in a manner to produce an output voltage which is less than the input voltage. The circuit incorporates a semiconductor switch, an LC filter to reduce the output voltage ripple, and a free-wheeling diode to ensure that the inductor current has a path to flow when the switch is open.

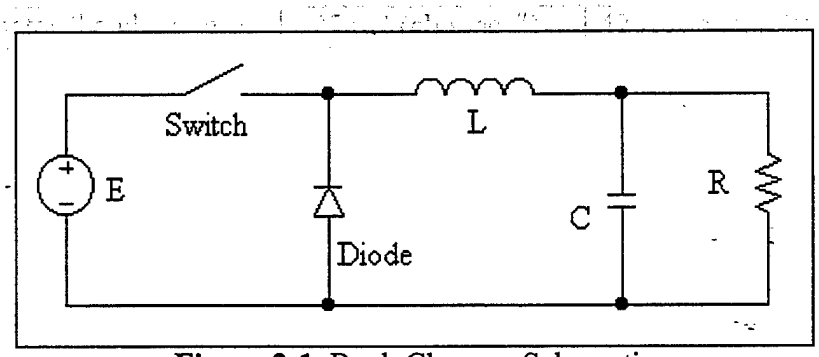


Figure 2-1, Buck Chopper Schematic

1. Basic Buck Chopper Topology

The topology for the buck chopper is shown in Figure (2-1). There are two modes of operation for the buck chopper depending on the current through the inductor. The primary mode of operation is characterized by the current through the inductor being continuous. In the other mode of operation the current through the inductor is discontinuous. At some point during a switching period for discontinuous operations the inductor energy is depleted as the current reaches zero and remains at zero until the source is reconnected to the inductor via the switch. The source reconnect marks the

beginning of the next cycle. Owing to its linear input-to-output characteristics and lower peak currents, it is attractive to design the buck chopper to remain in continuous inductor current mode for normal operating conditions. As a result, this thesis will focus on the continuous mode. A more detailed description of the discontinuous inductor current operation of the circuit is found in reference [3].

Referring to Figure (2-1), the DC power source voltage is E and the switch is operated at a constant frequency. When the switch is 'on', the diode is reverse biased and the inductor accumulates energy from the source. When the switch 'opens', the source is removed from the circuit and the free-wheeling diode provides a path for the inductor current which supplies its stored energy to the capacitor and the load. The ratio of the 'on-time' to the switching period is termed the duty cycle. The capacitor reduces the output ripple to an acceptable value, determined by the sensitivity of the load. In most cases, the AC ripple is much smaller than the DC output voltage, with a reasonable value being 0.5 % or less. The net result is that the LC low- pass filter passes the average of the switched voltage while eliminating the high-frequency switching harmonics. For notation purposes, capital letters will denote average value quantities while lowercase letters will denote instantaneous quantities. The switch and diode in the buck chopper circuit are assumed to be ideal for the following derivations. During the time that the switch is closed, the governing equations are:

$$E = v_L(t) + v_C(t) \tag{2-1}$$

$$E = L\frac{di_L(t)}{dt} + V_C \tag{2-2}$$

$$\frac{di_L(t)}{dt} = \frac{E - V_C}{L} \tag{2-3}$$

$$di_L(t) = \frac{E - V_C}{L} \cdot dt \tag{2-4}$$

$$I_{max} - I_{min} = \frac{E - V_C}{L} \cdot DT \tag{2-5}$$

where the value of the output capacitance is assumed to be large enough so that v_C is equal to V_C, the duty cycle of the switch is D, and the period of the switch is T. The assumption that the capacitor voltage is a DC value can be seen from:

$$v_C(t) = \tilde{v}_C(t) + V_C \tag{2-6}$$

where $\tilde{v}_C(t)$ is the capacitor AC ripple voltage and $\tilde{v}_C(t) << V_C$.

During the time that the switch is 'open', the equations which govern the circuit operation are:

$$0 = v_L - V_C \tag{2-7}$$

$$0 = L\frac{di_L}{dt} + V_C \tag{2-8}$$

$$\frac{di_L}{dt} = \frac{-V_C}{L} \tag{2-9}$$

$$di_L = \frac{-V_C}{L} \cdot dt \tag{2-10}$$

$$I_{min} - I_{max} = \frac{-V_C}{L} \cdot (1 - D) \cdot T \tag{2-11}$$

By equating Equations (2-5) and (2-11), an expression relating the input voltage to the output voltage may be derived:

$$V_C = D \cdot E \tag{2-12}$$

Typical waveforms for the buck chopper are illustrated in Figure (2-2). From the beginning of a period T until the time shown as DT, the switch is 'shut' and the current through the inductor, i_L , rises. The current through the switch, i_s , is identical to the inductor current while the switch is 'shut' so it also rises during this time interval. The diode is reverse biased so the diode current, i_D , is zero during this interval. The source voltage is connected to the input-side of the inductor while the capacitor is connected to the output-side of the inductor, so the inductor voltage v_L is seen as the difference between the two for this interval. When the switch 'opens', the source is isolated from the rest of the circuit and the free-wheeling diode provides a path for the inductor current to flow.

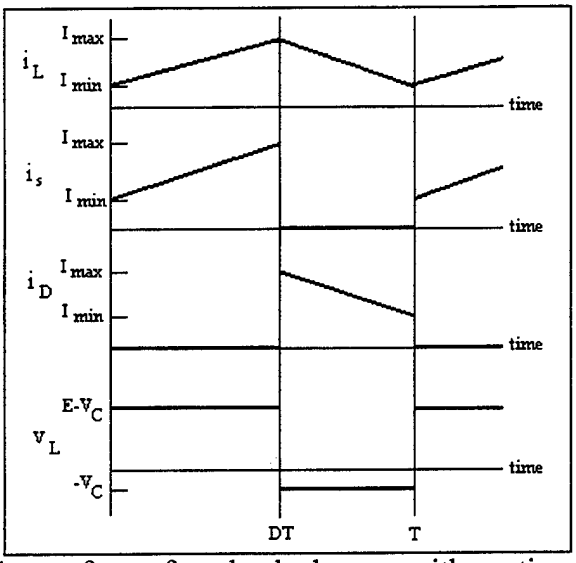


Figure 2-2, Typical waveforms for a buck chopper with continuous inductor current

During this interval the inductor current falls while the switch current is zero due to the switch being 'open'. The diode current is identical to the inductor current during

this interval. Finally, by applying Kirchhoff's voltage law to the loop which includes the inductor, diode and capacitor, and assuming zero voltage drop across the diode, the inductor voltage is seen to be equal to the opposite of the capacitor voltage. These waveforms should be referred to during the following discussion.

In order to select an inductor for the converter which is sufficiently large enough to maintain continuous current, an equation must be developed based on the circuit components and parameters. This development follows starting with the average inductor and load currents. The average load current is:

$$I_R = \frac{V_C}{R} = I_L = \frac{I_{max} + I_{min}}{2} \tag{2-13}$$

where the average inductor current is assumed to be equal to the average load current due to the large capacitor size. In other words, the DC current will flow exclusively through the resistor and the AC current will flow through the capacitor. The maximum inductor current is found by solving Equation (2-13) for Imax.

$$I_{max} = \frac{2V_C}{R} - I_{min} \tag{2-14}$$

Substituting Equation (2-14) into Equation (2-11) yields:

$$I_{min} - \frac{2V_C}{R} + I_{min} = \frac{-V_C}{L_{crit}} \cdot (1 - D) \cdot T \tag{2-15}$$

$$2I_{min} = \frac{-V_C}{L_{crit}} \cdot (1 - D) \cdot T + \frac{2V_C}{R} \tag{2-16}$$

By setting the minimum inductor current to zero, the value of the critical inductance is found:

$$L_{crit} = \frac{T \cdot R}{2} \cdot (1 - D) \qquad (2\text{-}17)$$

This minimum inductance value must be satisfied in order to ensure continuous current operation of the buck chopper.

2. Component Selection

For laboratory implementation the nominal duty cycle was selected to be 0.75 based on an input voltage of 400 V_{DC} and an output voltage of 300 V_{DC} using Equation (2-12). The operating frequency for the switch was selected as 17 kHz as a compromise between audible noise, switch power loss and filter component size. Switch power loss increases linearly with frequency while component sizes decrease. The resulting period of the switch is 59 μsec. A full power rating was determined to be 9 kW, a value large enough to demonstrate the PEBB concept but small enough to allow for laboratory construction and testing. A 10% load of 100 Ω was selected for determining the critical inductance which was found from Equation (2-17) to be 737 μH. In order to have a load-side filter with a very low resonant frequency, a 2000 μF capacitor was selected. The components utilized in constructing the circuit are summarized in Table (2-1).

Switch	International Rectifier IRGT1090U06 Insulated Gate Bipolar-Junction Transistor (IGBT), with antiparallel diode	
Capacitor	Sprague Powerlytic 2000 μF, 450 V_{DC}	
Inductor (hand wound)	760 μH (chopper#1)	860 μH (chopper#2)

Table 2-1, Circuit components

The combined switch and diode pack used in the buck chopper is a high-speed (25 to 100 kHz) and high-power (600 V, 90 A) device. As such, the voltage drop and switching loss

during steady-state operation are small compared to the voltages and currents being switched, thus justifying the assumption that the voltage drops across these components are zero for the equations derived in this chapter.

The main purpose of the load-side 2-pole inductor-capacitor (LC) filter of the buck chopper is to eliminate any switching harmonics (17 kHz) that otherwise would be passed to the load. The low-pass filter also acts to decouple the primary rectified voltage to the secondary DC bus line. The transfer function of this filter is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{LCs^2 + \frac{L}{R}s + 1}. \qquad (2\text{-}18)$$

When the values of Table (2-1) are substituted into the transfer function, the Bode plots for the buck chopper operating at 100% load and 10% load are computed and plotted.

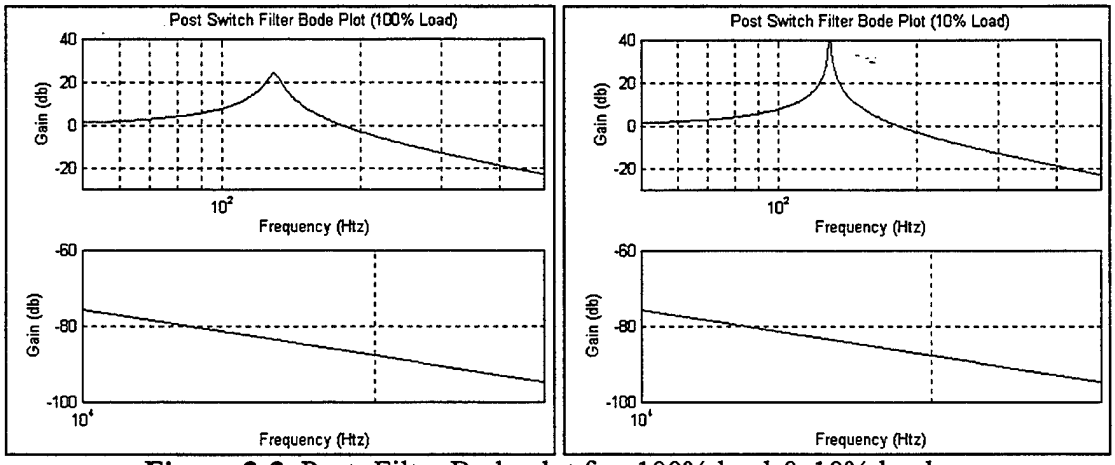


Figure 2-3, Post- Filter Bode plot for 100% load & 10% load

Figure (2-3) illustrates how the 17kHz switching noise is attenuated by 80 dB and how the input 360 Hz ripple is attenuated by 18 dB at the load for load resistances in the range $10\Omega \leq R_L \leq 100\Omega$. It should be noted that due to the relative size of the

capacitance as compared to the filter inductance and load resistance, variations in load resistance between $10\Omega \leq R_L \leq 100\Omega$ have negligible effect on the overall Bode plot.

To further ensure no input-to-output communication of the 360 Hz input voltage ripple, a prefilter is used to decouple the source from the buck chopper. The values of the components were selected to further reduce the ripple from the rectifier bank while maintaining some commonality. Hence a 2000μF computer grade electrolytic capacitor along with Arnold's toroid core for the hand-wound inductor were used in the prefilter.

Capacitor	Sprague Powerlytic 2000 μF, 450 V_{DC}	
Inductor (hand wound)	425 μH (chopper#1)	425 (chopper#2)

Table 2-2, Prefilter Circuit Components

Substituting these values into Equation (2-18) results in the following Bode plots:

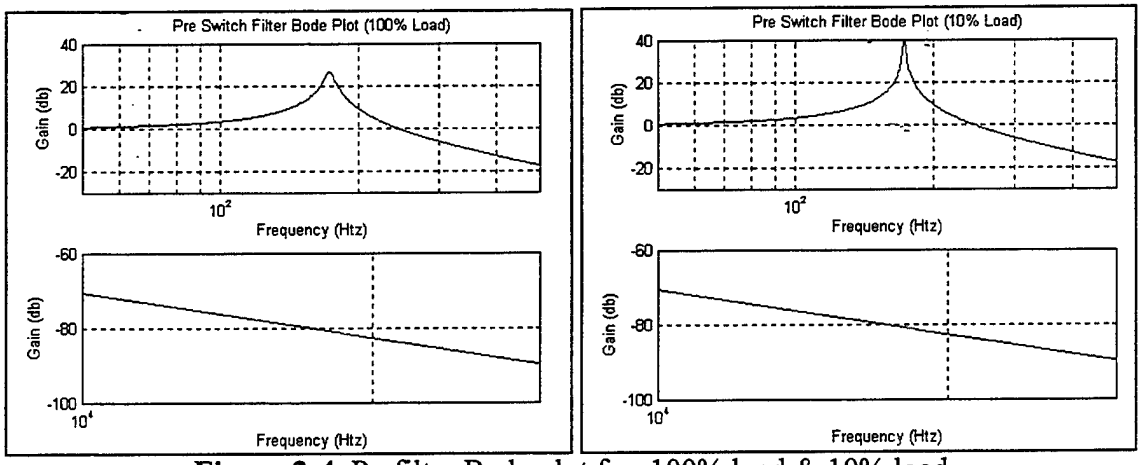


Figure 2-4, Prefilter Bode plot for 100% load & 10% load

As can be seen in both Figures (2-4), the source three-phase 360 Hz ripple is attenuated 10.65 dB at the input to the switch and across Cf (Figure (2-5)). The expanded topology of the buck chopper including the prefilter is documented in Figure (2-5) while the pertinent information on the filters is recorded in Table (2-3).

	Prefilter (10%<PL<100%)					Output filter (10%<PL<100%)				
	fres	L	C	G 360Hz	G(f=17 kHz)	fres	L	C	G 360Hz	G(f=17 kHz)
	Hz	μH	mF	dB	dB	Hz	μH	mF	dB	dB
Buck #1	172	425	2	-10	-79	129	760	2	-17.9	-87
Buck #2	173	425	2	-10	-79	120	875	2	-18.8	-86

Table 2-3, Summary of filter component values and filter performance

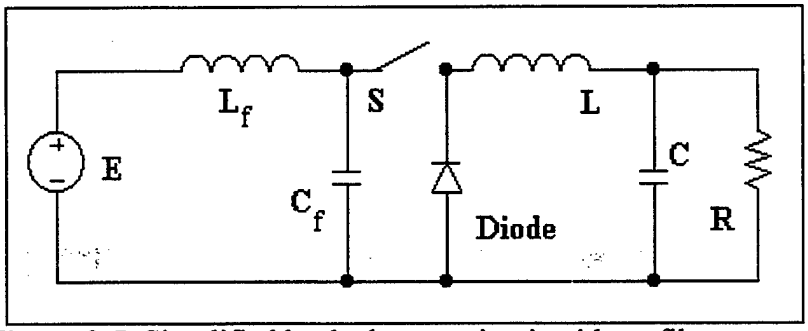


Figure 2-5, Simplified buck chopper circuit with prefilter

B. IGBT DRIVER CIRCUIT

The main switch used in the construction of the power section requires a set of input voltages on the gate terminal which are properly controlled in magnitude with a relatively high value of pulse source and sink current in order to operate properly. The circuit constructed for use with the IGBT is shown in Figure (2-6).

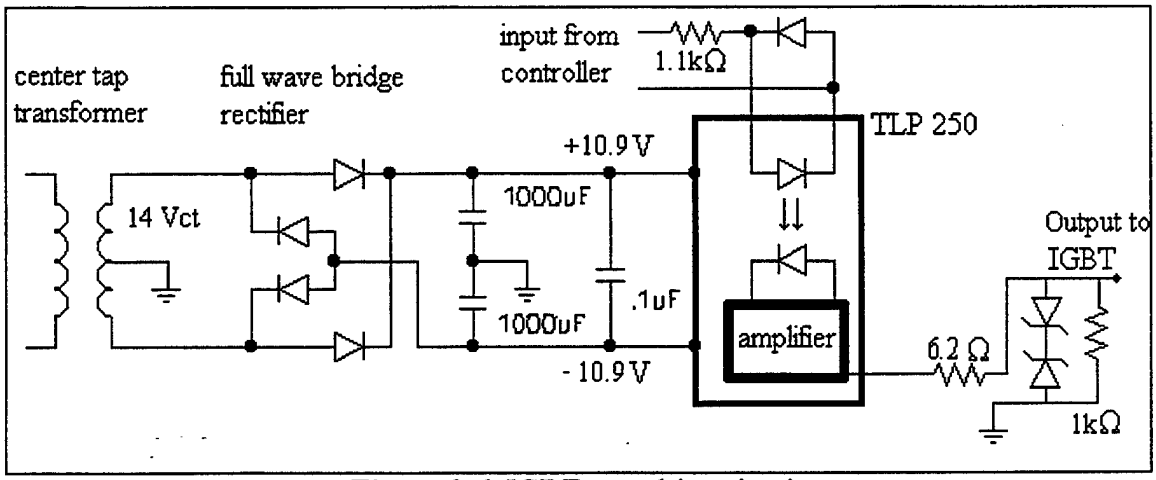


Figure 2-6, IGBT gate drive circuit

The heart of the driver circuit is the TOSHIBA TLP 250 gate drive photo IC coupler. This device combines the high speed, high gate current, and optical isolation of the control circuit in one package for ease of use. The 120/14 V_{AC}, center-tap transformer, diode configuration, and 1000 μF capacitors produce an unregulated ±10 VDC power supply which has a floating ground. The 0.1 μF capacitor reduces any high-frequency noise seen on the power supplies as a result of switching transients on the TLP 250. The high-speed diode and resistor connected to the TLP 250 diode allow for proper current to be sent to the TLP 250 photodiode. The zener diodes prevent the voltage on the IGBT gate from becoming too large thus protecting the gate circuit from damage. Finally, the output resistor ensures proper impedance matching of the IGBT gate and driver circuit while providing current limiting to the TLP 250 output transistors.

The operation of the circuit is straightforward. A 15 V input to the driver circuit will cause the LED on the TLP 250 chip to assume the 'on' state. The optical sensor within the chip will detect the condition of the diode and cause the output amplifier on the chip to set the voltage on the IGBT gate 'high' at + 10 V, thus turning it 'on'. Use of the optical isolator allows the output signal to float up to the switch voltage while the input signal remains at an isolated ground. The stray capacitance, associated with the IGBT gate circuit and leads between the IGBT and driver circuit, is rapidly charged due to the high source current capability of the TLP 250 output amplifier.

When the input voltage to the driver circuit is set to -15 V, the TLP 250 diode is turned 'off', and the output amplifier will set the gate voltage to -10V. Once again, the current sinking ability of the output amplifier enables the charge on the IGBT gate to be

removed very rapidly, enhancing the ability of the driver to be used in higher speed circuit applications.

C. POWER SECTION TEST RESULTS

The power section was tested at frequencies ranging from 5 kHz to 27 kHz and power levels from ranging 10% to 145% rated power (9 kW @ 100%). The switching and diode loss from the IGBT pack was less than 200 W at full power, as measured from the input and output voltage and current values. This required that the IGBT be mounted onto a Delta NC-421 semiconductor heat sink[10]. The natural convection dissipation capabilities of the heat sink are shown Figure (2-7). Operation of the IGBT's above 55% of the rated power of the buck chopper generates more heat than the sink can dissipate by natural convection. Thus, heat removal capacity was quadrupled by the addition of two Globe model A-47-B15a-15T3-000 muffin fans with rated flow of 26 cf./min. The addition of the muffin fans was required for sustained operations above 55% rated power. Further consideration of the over-temperature condition will be developed in Chapter III.

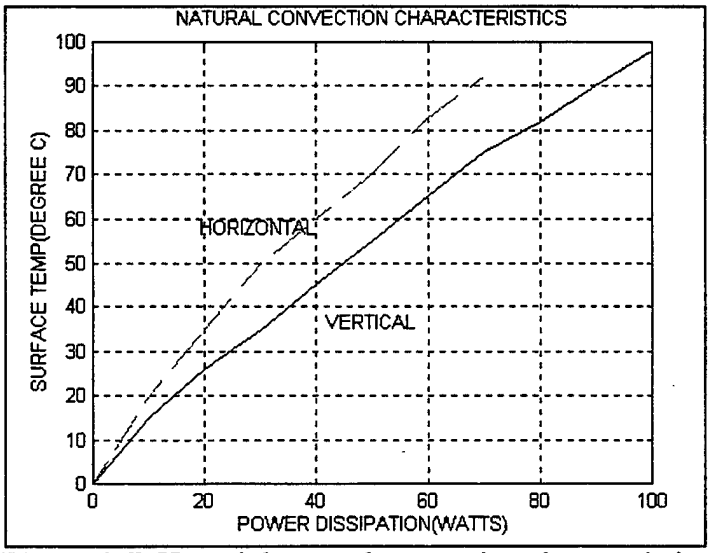


Figure 2-7, Heat sink natural convection characteristics

Figure (2-7) shows two curves representing the power dissipation capabilities of the heat sink. The curve labeled horizontal applies to the heat sink when the sink is mounted in the horizontal position while the curve labeled vertical applies when the sink is mounted in the vertical position. To maximize the capability to remove heat, the sink was mounted in the horizontal position.

Circuit stability for all conditions tested was verified and the inductor current was found to be continuous at all loads greater than 10%. Operation of the driver circuit was acceptable for all frequencies tested from 5 kHz to 30 kHz, with the supply voltages ranging from ± 5 to ± 15 V. The audio output at frequencies below 17 kHz was substantial, justifying the choice for the switching frequency of the controller to be at or above 17 kHz. In addition, switching losses above 17 kHz would require the addition of further heat sinking.

D. CORE SIZING

A properly sized core is integral to the proper operation of the buck chopper for the desired output power range. Failure to identify the correct switching frequency can lead to significant reductions in actual inductance that, if not accounted for, could cause the switch to fail from over-current due to core saturation at high-power levels. An iterative procedure to size the core starts with selecting a switching frequency[11]. If the frequency of the chopper is variable, then the range must accompany the following calculations. With minimum inductance calculated in Equation (2-17), the number of turns (N) on a specific core is obtained from:

$$N = 1000\sqrt{L / L_{1000}} \qquad (2\text{-}19)$$

Where the value L_{1000} is a manufacturer supplied value that represents the inductance that could be achieved if the core was wrapped with 1000 turns of wire and L is the desired inductance. Using a standard table[9], the wire gauge is selected based on the calculated maximum inductor current. The calculated peak current of 33.5 Amps yields a 10 gauge wire size. With this known, the maximum number of turns on the core is derived from the manufacturer provided data sheet. If the calculated number of turns is greater than the maximum wrap data, a larger core is required. Figure (2-8) shows a typical manufacturer provided data sheet.

PHYSICAL SPECIFICATIONS

CORE DIMENSIONS	INCHES			MILLIMETERS		
	O.D.	I.D.	HT.	O.D.	I.D.	HT.
NOMINAL	3.069	1.938	0.500	77.8	49.2	12.70
	3.063	1.938	0.560	77.8	49.2	14.22
AFTER FINISH	3.108	1.888	0.550	78.9	48.0	13.97
	3.108	1.888	0.610	78.9	48.0	15.49
	MAX.	MIN.	MAX.	MAX.	MIN.	MAX

MEAN LENGTH OF MAGNETIC PATH (l)			CROSS SECTIONAL AREA OF MAGNETIC PATH (A)		APPROXIMATE WEIGHT OF FINISHED CORE	
CORE HT.	IN.	CM.	IN^2	CM^2	LBS.	GRAMS
.500	7.87	20.0	0.274	1.77	0.64	290
.560	7.87	20.0	0.308	1.99	0.66	300

MEAN LENGTH OF TURN FOR FULL WINDING

CORE HEIGHT	IN.	CM.
0.600	2.36	5.99
0.560	2.49	6.32

ELECTRICAL SPECIFICATIONS

CORE SPECIFICATIONS				WINDING DATA FOR FULL-WOUND CORE		
PART NUMBER	NORM PERM. μ	IND mH FOR 1000 TURNS	NOMIN DC RESIST OHMS PER mh	AWG WIRE SIZE	TURNS	DC RESISTANCE OHMS
219233	205	233	0.0052	12	271	0.098
133197	173	197	0.0062	13	339	0.141
156167	147	167	0.0073	14	424	0.221

Figure 2-8, Manufacturer's provided data sheet[11]

With the correct core size chosen and the number of turns (N) computed, the maximum flux density (Bmax) in Gauss is calculated according to the following equation:

$$B_{max} = \frac{E_{rms} \cdot \times 10^8}{4.44ANf} \qquad (2\text{-}20)$$

Core area (A) in cm^2 is determined from the manufacturer's data sheet (Figure (2-8)), Erms is the equivalent sinusoidal rms voltage across the coil and f is the switch frequency in Hz. Erms is the output voltage of the chopper and occurs during the period when the switch is off. The magnetizing force (H in oersteds) is determined from the following equation:

$$H = \frac{0.4\pi NI_{max}}{l} \qquad (2\text{-}21)$$

Where l, the mean magnetic path in cm, is provided by the manufacturer's data sheet. Imax can be derived by computing (Imax - Imin) via Equation (2-5) and uncovering the average load current. Equation (2-5) yields 5.8 amps and the average load current is 30 amps at 100% output power. Imax can be calculated by substituting those values into the following equation:

$$I_{max} = I_{avg} + \frac{I_{max} - I_{min}}{2} \qquad (2\text{-}22)$$

With maximum flux density and magnetizing force computed from Equations (2-20) and (2-21), the relative permeability is computed according to:

$$\mu = \frac{B}{H} \qquad (2\text{-}23)$$

This value represents the minimum permeability that the core must have in order to remain non-saturated and must be compared with the permeability μ computed from the test core correlation equations:

$$\mu = \frac{Lx10^9}{11.7[\log_{10}\frac{od}{id}]h_eN^2} \quad (2\text{-}24)$$

where the effective core height in cm is:

$$h_e = h - \frac{1.717r^2}{od - id} \quad (2\text{-}25)$$

Core height 'h', outside diameter 'od', inside diameter 'id' and radius 'r', all in cm, are provided in the manufacturer's data sheet (Figure (2-8)). The core permeability will degrade due to the principle of Incremental Permeability which is caused by a superimposed DC biasing current and results in a lower relative permeability. This is computed by applying the results of Equation (2-24) to Figure (2-9).

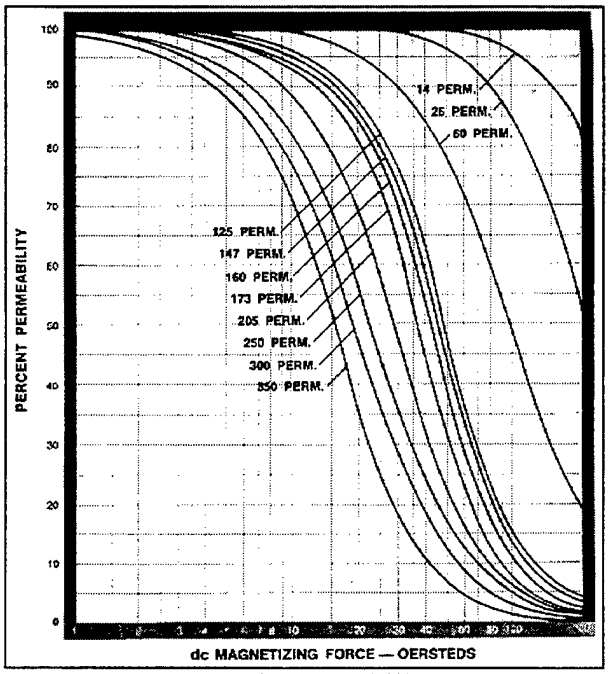


Figure 2-9, Incremental Permeability vs. DC Bias[11]

By showing that the core permeability after incremental losses is greater than the conditional permeability computed from Equation (2-23), a proper size core has been selected. In addition, to ensure peak efficiently of the inductor, Q, the ratio of reactance to the effective resistance, should be maximized. Q can be optimized by reviewing the manufacturer's provided curves, such as that one shown in Figure (2-10), and selecting a core with the peak Q in the vicinity of the operating frequency.

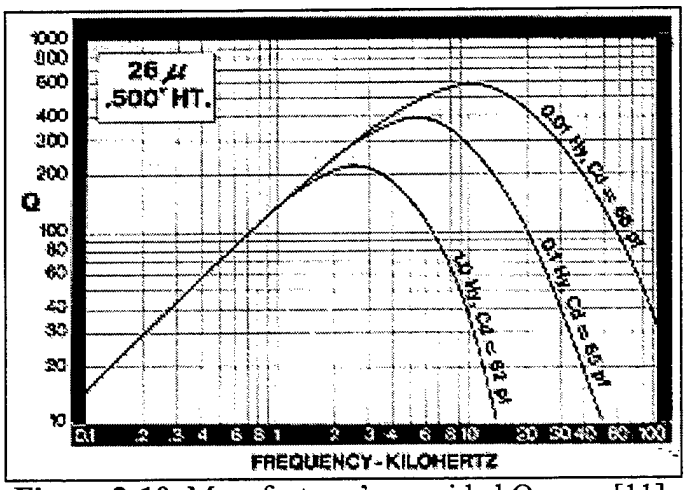


Figure 2-10, Manufacturer's provided Q curve[11]

Upon selecting the core using the procedure outlined above, the predicted inductor losses are computed. The first aspect of inductor loss is the DC winding resistance, which is computed by:

$$R_{dc} = \frac{l_w N R}{12000} \tag{2-26}$$

where l_w is the mean length of each turn in inches (available from Figure (2-8)) and R is the resistance per 1000 feet of wire to be used. In addition to the normal DC resistance of a winding, there exists an incremental change in the winding resistance due to the skin

effects of an AC current. The following equation can be used to approximate the ratio of the AC to DC resistance:

$$\frac{Rac}{Rdc} = .96 + .00335x^2 - .000038x^3 \qquad (2\text{-}27)$$

$$x = d\sqrt{\frac{f}{(1+.00393(T-20))}} \qquad (2\text{-}28)$$

where f is the frequency in hertz, d is the wire diameter in inches and T is the temperature measured in degrees Celsius. By applying the value determined in Equation (2-28) to this ratio, the AC resistance is determined. The next step is to compute actual core losses using Legg's equation:

$$R_{ac(core)} = \mu L f(aB_{max} + c + ef) \qquad (2\text{-}29)$$

The values for the coefficients are provided with most manufacturer's specifications sheet and are summarized in Figure (2-11). Bmax is computed using Equation (2-20).

SPECIFCATIONS				TYPICAL VALUES		
MAXIMUM CORE LOSS		TEST				
Rac/L Ω/H	FLUX DENSITY GAUSS	FREQ HZ	PERM μ	HYSTERESIS LOSS COEF A x(10E-6)	RESIDUAL LOSS COEF C x(10E-6)	EDDY CURRENT LOSS COEF E x(10E-9)
0.25	20	1800	300	1.1	30	43
0.25	20	1800	250	1.2	28	37
0.25	20	1800	205	1.3	25	30
0.20	20	1800	173	1.4	25	25
0.20	20	1800	160	1.5	25	22
0.20	20	1800	147	1.6	25	20
0.20	20	1800	125	1.6	25	13
1.50	10	8000	60	3.2	50	10
7.0	4	75000	26	8.0	96	7.7

Figure 2-11, Electrical specifications and typical loss coefficients[11]

The total power loss is the summation of the three calculated losses as follows:

$$P_{Loss} = I_{avg}^{2} R_{dc} + I_{rms}^{2} (R_{ac} + R_{ac(core)}) \quad (2\text{-}30)$$

E. PHYSICAL LAYOUT

Design specifications called for the following criteria:

- Minimum output power: 9 kW
- Switching frequency: 5-30 kHz
- Input / Output: 400V (23 A) input and 300 V (30 A) output
- Input filter resonance: 172 Hz
- Continuous operations: loads > 10%

Based on these values and subsequent testing, the resulting source-side DC-to-DC converters operate at a rated output power of 9 kW and a switching frequency of 17 kHz. The basis for component selection stems from the design specifications given above.

Table (2-4) summarizes theoretical steady-state performance. Parameter definitions are included with the topology overview. These parameters form the basis of component sizing and selection. Since 2 large cores already existed from previous research, only one set of cores were needed for completion of both buck choppers. Since the two source choppers contain different size inductors, Table (2-4) provides data for both converters.

From the specifications and data from Table (2-3), 600 V / 90 A IGBTs were selected based on their high current density, rugged design, and simple gate-drive. An

IGBT and diode pair comprise each module allowing collocation of the switch and diode components of the buck converter topology. The data sheets for the IGBT are provided in Appendix [A].

	Value	
Parameter	Buck Converter #1	Buck Converter #2
Pout	9.00 kW	9.00 kW
E	400.00 V	400.00 V
Vc	300.00 V	300.00 V
f_{switch}	17.00 kHz	17.00 kHz
f_{line}	360.00 Hz	360.00 Hz
Output filter f_o	129.09 Hz	120.31 Hz
Input filter f_o	172.63 Hz	172.63 Hz
d	0.75	0.75
L_{crit}	735.29 uH	735.29 uH
L	760.00 uH	875.00 uH
Input filter L	425.00 uH	425.00 uH
C	2000.00 uF	2000.00 uF
Full Load I_{lavg}	30.00 A	30.00 A
Full Load I_{lmax}	32.90 A	32.52 A
Full Load I_{lmin}	27.10 A	27.48 A
Full Load ΔI_L	5.80 A	5.04 A
10% Load I_{lavg}	3.00 A	3.00 A
10% Load I_{lmax}	5.90 A	5.52 A
10% Load I_{lmin}	0.10 A	0.48 A
10% Load ΔI_L	5.80 A	5.04 A

Table 2-4, Summary of component size and operating parameters

In order to achieve low output ripple while overcoming component heating concerns, 2000 uF electrolytic capacitors were chosen. In addition to filtering the output of the source-side DC-to-DC converters, these capacitors were also used in the input LC low-pass filters with 425 uH inductors. Input filtering was designed to decouple the buck converter from the source.

Two forms of protection are provided by the controller. IGBT thermal protection is provided by over-current time-out utilizing the output current. Additionally, peak current protection of the IGBT is accomplished by a pulse-by-pulse monitoring of the inductor current. The pulse-by-pulse feature protects the IGBT from over-current spikes by disabling the switch when high current peaks occur. This feature is quick acting. As a result, once the immediate danger of the current spike is gone, the slower over-current time-out takes over and shuts down the circuit.

Input, output and common plug connections are incorporated using ceramic terminal blocks for each buck chopper. The physical layout of the power section is shown in Figure (2-12). Cooling holes in the aluminum base plate, not visible in Figure (2-12), allow air flow from the cooling fans.

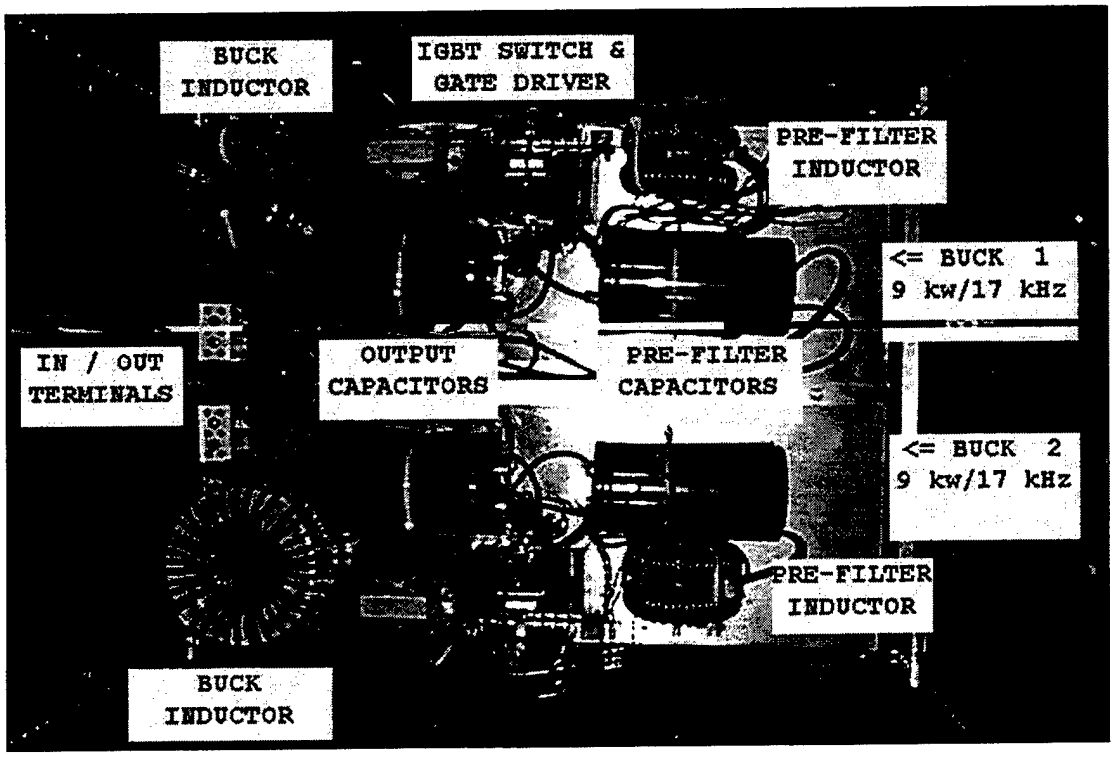


Figure 2-12, Supply-side buck chopper physical layout

With the source-side buck choppers constructed and tested, the next step is to develop the controller. This will be detailed in Chapter III.

III. CLOSED-LOOP FEEDBACK WITH FEED-FORWARD

A. BASIS FOR OPERATION

Four different control algorithms for the buck chopper were evaluated in a previous thesis at NPS[4]. These included linear feed-forward, integrator-based feedback, multiloop feedback and state difference feedback. The previous research work concluded that state difference feedback provided excellent performance and satisfied stability conditions for a wide variety of loads. Thus, a variation of state difference feedback which included a feed-forward loop, a house curve and two methods of protection was used to control the buck choppers. The feed-forward loop compensates for input voltage variations and the house curve guarantees current sharing when the converters operate in parallel.

1. Theory of Operation

All of the rest of this section on Theory of Operation is taken from Smedley [1],

...a switch operates according to the switch function k(t) at a frequency $f_s=1/T_s$,

$$k(t) = \begin{cases} 1 & 0 < t < T_{ON} \\ 0 & T_{ON} < t < T_s. \end{cases} \qquad (3\text{-}1)$$

In each cycle, the switch is on for a time duration T_{ON} and is off for a time duration T_{OFF} , where $T_{ON}+T_{OFF}=T_s$. The duty-ratio $d=T_{ON}/T_s$ is modulated by an analog control signal $v_{ref}(t)$. The switch input signal x(t) is chopped by the switch. The frequency and pulse width of the switch output y(t) is the same as that of the switch function k(t), while the envelope of y(t) is x(t)...

$$y(t) = k(t) \cdot x(t) \qquad (3\text{-}2)$$

With the switch closed, the chopper is governed by the following equations:

$$\frac{dv_c}{dt} = \frac{1}{C}(i_L - \frac{v_c}{R}) \tag{3-3}$$

$$\frac{di_L}{dt} = \frac{1}{L}(e - V_c) \tag{3-4}$$

With the switch S open the following equations govern the operation of the buck chopper.

$$\frac{dv_c}{dt} = \frac{1}{C}(i_L - \frac{v_c}{R}) \tag{3-5}$$

$$\frac{dil}{dt} = \frac{1}{L}(0 - V_c) \tag{3-6}$$

With d already defined as the fractional interval that switch S is closed. This is now a time varying interval, and a lowercase letter is used in contrast to the static case in which D was used. The fractional interval that the switch is open is *d'*(1-*d*).The next step is to with the equations according to the relative time the circuit is in each sta. Thus Equations (3-3) and (3-5) are multiplied by d to obtain:

$$d\left(\frac{dv_c}{dt}\right) = \frac{d}{C}(i_L - \frac{v_c}{R}) \tag{3-7}$$

$$d'\left(\frac{dv_c}{dt}\right) = \frac{d'}{C}(i_L - \frac{v_c}{R}) \tag{3-8}$$

If the two equations are added and $d+d'=1$ is noted, the result is that of:

$$\frac{dv_c}{dt} = \frac{1}{C}(i_L - \frac{v_c}{R}) \tag{3-9}$$

Similarly Equations (3-4) and (3-6) are modified in a like manner to obtain Equations (3-10) and (3-11).

$$d\left(\frac{di_L}{dt}\right) = \frac{d}{L}(e - V_c) \tag{3-10}$$

$$d\left(\frac{di_L}{dt}\right) = \frac{d'}{L}(0 - V_c) \tag{3-11}$$

These two equations are added to obtain:

$$\frac{di_L}{dt} = \frac{1}{L}(de - V_c) \tag{3-12}$$

The resulting equation is a junction of the switch duty cycle; this contrasts with Equation (3-9) which does not depend upon *d*.

The next step in the development process is to introduce a small-signal component to each variable, which is represented by a fixed value portion a small signal portion. The following notation '^" is used to represent the small-signal portion.

$$e = E + \hat{e} \tag{3-13}$$

$$i_L = I_L + \hat{i}_L$$

$$v_c = V_c + \hat{v}_c$$

$$d = D + \hat{d}$$

$$d' = (1 - D) - \hat{d}$$

$$i_s = I_s + \hat{i}_s$$

$$\frac{di_L}{dt} = \frac{d\hat{i}_L}{dt}$$

$$\frac{dv_c}{dt} = \frac{d\hat{v}_c}{dt}$$

$$i_c = 0 + \hat{i}_c$$

$$i_R = I_R + \hat{i}_R$$

The relations of Equation (3-13) are then substituted into Equations (3-9) and (3-12) to obtain:

$$\frac{d\hat{v}_c}{dt} = \frac{1}{C}(I_L + i_L - \frac{V_c}{R} - \frac{\hat{v}_c}{R}) \tag{3-14}$$

$$\frac{d\hat{i}_L}{dt} = \frac{1}{L}((D + \hat{d})(E + \hat{e}) - V_c - \hat{v}_c) \tag{3-15}$$

That there are zero-, first-, and second order terms allows us to simplify the equations. The second order terms, which are products of two small-signal terms, can be dropped in consideration of their relative size. Equations (3-14) and (3-15) become:

$$\frac{d\hat{v}_c}{dt} = \frac{1}{C}(I_L - \frac{V_c}{R} + \hat{i}_L - \frac{\hat{v}_c}{R}) \tag{3-16}$$

$$\frac{d\hat{i}_L}{dt} = \frac{1}{L}(DE - Vc + E\hat{d} + D\hat{e} - \hat{v}_c) \tag{3-17}$$

These equations can be separated into two sets of equations. The first represents the fixed part of the equations, and the second set the small-signal portion. The fixed portion is given by:

$$0 = \frac{1}{C}(I_L - \frac{V_c}{R}) \tag{3-18}$$

$$0 = \frac{1}{L}(DE - V_c) \tag{3-19}$$

Substituting Equation (3-18) into Equation (3-16) and Equation (3-19) into (3-17), the second set of small-signal equations become:

$$\frac{d\hat{v}_c}{dt} = \frac{1}{C}(\hat{i}_L - \frac{\hat{v}_c}{R}) \tag{3-20}$$

$$\frac{d\hat{i}_L}{dt} = \frac{1}{L}(E\hat{d} + D\hat{e} - \hat{v}_c) \tag{3-21}$$

A circuit model, which is represented by the above equations, is shown in Figure (3-1). This figure simultaneously includes the zero -order and first order terms from the preceding equations.

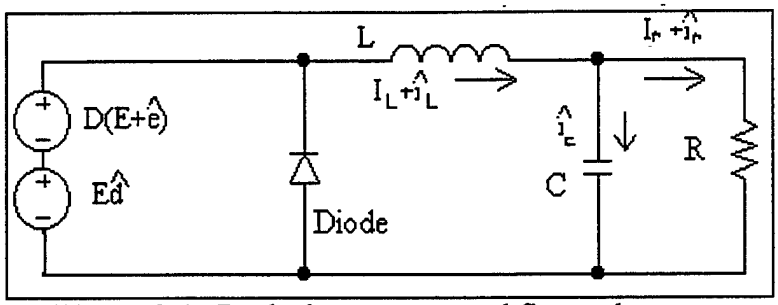


Figure 3-1, Buck chopper zero and first-order terms

The open-loop frequency response of a buck chopper is needed to design a complete closed-loop system successfully. The analysis that follows applies to the idealized buck chopper that has only the minimum number of ideal circuit elements. There are no parasitic elements such as inductor resistance or series capacitor resistance included in the ideal model.

In Figure (3-1), the small-signal analysis for the output response to perturbations in duty cycle $\hat{d}$ is desired. Accordingly, all DC quantities established in Equations (3-18) and (3-19) may be ignored. Further, since only output voltage variations due to $\hat{d}$ are needed for a first look at open-loop characteristics, the perturbations in input voltage, $\hat{e}$, are set to 'zero' in Equation (3-21). This allows simplification of the circuit to that shown in Figure (3-2).

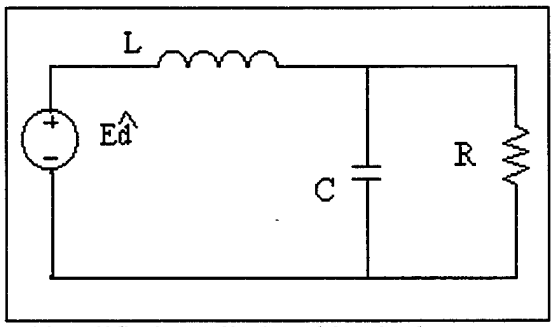


Figure 3-2, Simplified small-signal buck chopper representation

The linear transfer function of the system is:

$$\frac{\hat{v}_c(s)}{\hat{d}(s)} = \frac{E}{LCs^2 + \frac{L}{R}s + 1} = EF(s). \tag{3-22}$$

Where E,L,C and R are constants. If the converter output voltage is used as the feedback variable, then the output can be made to follow some input command. The circuit shown in Figure (3-3) mimics such a system. For this arrangement, the system 'error' is given by Equation (3-23).

$$v_e = v_i - v_c \tag{3-23}$$

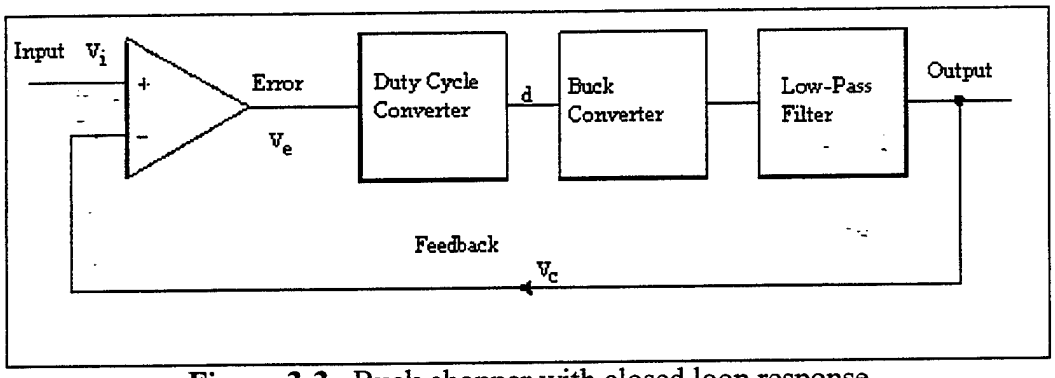


Figure 3-3, Buck chopper with closed loop response

The 'Duty Cycle Converter' relates system error to duty cycle, and is assumed to be an integrator as per Equation (3-24).

$$\hat{d} = \frac{K}{s}\hat{v}_e. \tag{3-24}$$

Thus, the control effort continues to operate until the error is driven to zero. Combining Equations (3-22), (3-23) and (3-24), and solving for $\hat{v}_c$ results in:

$$\hat{v}_c = EF(s)\hat{d} = (EF(s))\frac{K}{s}(\hat{v}_i - \hat{v}_c). \tag{3-25}$$

Figure (3-4) is the block diagram representation of Equation (3-25).

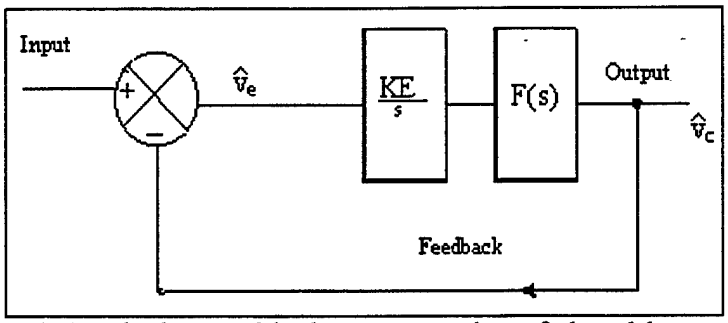


Figure 3-4, Buck chopper block representation of closed-loop response

The closed-loop response is given as follows:

$$\frac{\hat{v}_c(s)}{\hat{v}_i(s)} = \frac{G}{1+G} \tag{3-26}$$

where:

$$G = \frac{\hat{v}_c}{\hat{v}_e} = EF(s))\frac{K}{s}. \tag{3-27}$$

The overall gain must be set so that the system gain peak at the LC resonant frequency does not cause loop instability and there exists sufficient gain and phase margin. If the resonant peak is removed, the overall system gain can be increased and system performance improved.

2. State-Space Representation

The state-space representation of the buck chopper is useful in simulating transient response. To develop a continuous-time state-space representation of the buck chopper, the inductor current must be assumed continuous. Equations (3-3) and (3-4)

define the operation of the buck chopper circuit. These equations can be expressed in the following state-space form.

$$\dot{x} = Ax + Bu \tag{3-28}$$

where the state vector contains the variables

$$x = \begin{bmatrix} i_L \\ V_c \end{bmatrix} \tag{3-29}$$

and the derivatives of the state variables are:

$$\dot{x} = \begin{bmatrix} \frac{\partial i_L}{\partial t} \\ \frac{\partial V_c}{\partial t} \end{bmatrix} \tag{3-30}$$

and the input vector is:

$$u = \begin{bmatrix} E \\ 0 \end{bmatrix} \tag{3-31}$$

The system matrix is defined as:

$$A = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{3-32}$$

and the input matrix is:

$$B = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix} \tag{3-33}$$

The output of the system can be expressed as a linear combination of the states and the inputs

$$y = Cx + Du \tag{3-34}$$

3. Feed-Forward Control

The simplest method of control is based on Equation (3-35) for the steady-state duty cycle as depicted in Figure (3-5) . The duty cycle is determined from the ratio of the desired output voltage to the input voltage. This desired output voltage is the reference voltage in all control schemes investigated. Although feed-forward can achieve good steady-state regulation in low-loss buck choppers, the control scheme fails to achieve acceptable control with load transients. A small change in the load can cause the output filter to resonate and create large voltage peaks [4]. The feed-forward control does, however, decouple variations in the input voltage to the output of the buck chopper. Thus, this feature makes the feed-forward a highly desirable component of the final control scheme.

$$D = \frac{V_{out}}{V_{in}} = \frac{V_c}{E} \tag{3-35}$$

The state-space representation of the buck chopper is useful in simulating transient performance as will be discussed in Chapter IV.

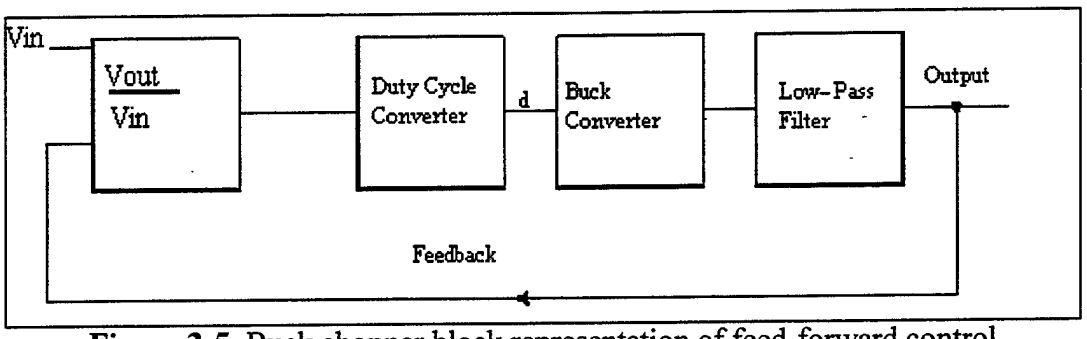


Figure 3-5 Buck chopper block representation of feed-forward control

4. Integrator-Based Feedback

An integrator control can achieve zero-voltage regulation which is not possible with linear feed-forward control. The integrator control functions by first creating an error signal based on the difference between input voltage and the reference voltage. The integral of the error signal then becomes the commanded duty cycle (Figure 3-6).

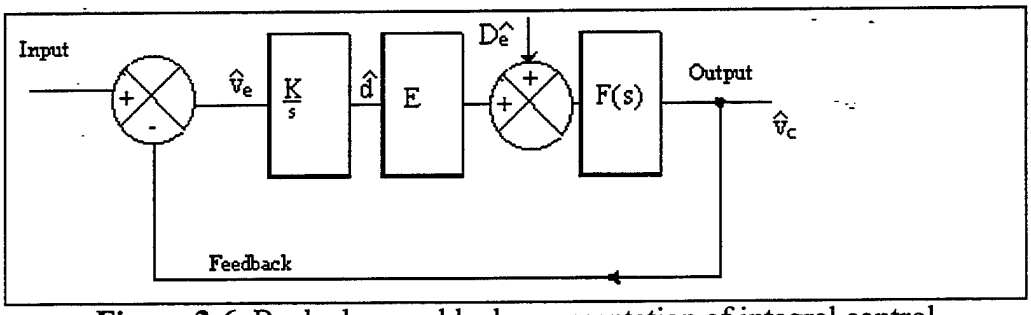


Figure 3-6 Buck chopper block representation of integral control

Therefore, if the output voltage is different from the reference voltage the duty cycle is changed until the error reaches zero. The integrator control will compensate for nonlinear elements that introduce a relatively fixed bias into the required duty cycle. Non-ideal switching components, such as the IGBT and freewheeling diode, have small voltage drops when conducting. These voltage drops will result in a voltage signal at the input to the output filter that is lower than predicted. The output voltage will also reflect this

reduction. The control eliminates this problem by providing an ordered duty cycle that includes the required bias in order to overcome these voltage reductions. The integrator does not decouple the input source as does the feed-forward method of control. To reduce the effect of the coupling, the integrator gain is sufficiently low as not to reduce the damping of the buck chopper circuit. This prohibits the controller from responding quickly to load changes. Additionally, with the input coupled to the output, any change in the input voltage will result in an immediate increase that is proportional to the value of the duty cycle at the time of the voltage change multiplied by the change in the input.

The transient response of the buck chopper with integrator control is similar to that of the feed-forward control method [4]. The method suffers from the stimulated resonance of the buck chopper filter circuit. Yet, the advantage of zero-voltage regulation makes it favorable as a component in a more complex control scheme. The response may even be further improved through the use of both voltage and current errors in the integral control. This complex control scheme will be developed in a later section.

5. Multiloop

The transient response of both the feed-forward and integrator control scheme is unacceptable. Both methods failed in their ability to adequately control the overall natural frequencies of the system. Multiloop involves the feedback of more than one signal. It offers an enhanced ability to control the system and reduces the effects of the LRC network by including both state variables, i_L and v_c. In ref. [4] a control scheme was studied that used the control law:

$$d(t) = D_{ss} - \left(h_v + h_n \int dt\right)\left[v_c - v_{ref}\right] - h_i i_L \qquad (3\text{-}36)$$

After gains were optimized by proper pole placement, the multiloop control scheme test results showed significant improvement in transient response when compared to simple feed-forward or integrator-based design. The oscillations that did follow load changes were significantly attenuated by the multiloop control scheme. However, the ability of multiloop control to minimize load transient peaks was considered inadequate. The two feedback parameters used, inductor current and output voltage, lag the output current transient event which caused excessive overshoot and undershoot in the voltage. To achieve quick output transient response without voltage sags, this scheme must be made extremely sensitive. To do so, would require increasing the system gains to a level that even minute changes in measured parameters or noise induced currents would cause instability.

6. State Difference

The state difference method offers improved transient response over the multiloop. To achieve the improved transient response, output current was included in the control algorithm. While the multiloop control was driven by a voltage error signal and variations in inductor current, both voltage error and current error signals are generated with the state difference control model. The specific error signals are $\left(i_L - i_o\right)$ and $\left(v_c - v_{ref}\right)$. The duty cycle now responds immediately to any mismatch between inductor

current and the output current. This difference represents the change in load current. In addition, the duty cycle is driven to minimize the difference between voltage error and load current error.

A house curve, necessary for parallel operations of two buck choppers, is implemented by inserting a load sensitive term into the small-signal portion of the control equation. At higher loads, the current term acts to introduce a larger negative small-signal term. This has the overall effect of lowering the duty cycle which, in turn, lowers the output voltage. By introducing a scaled current signal term into the integral and proportional term, the control equation will show immediate response to changes in load and the integral portion will drive the signal error to zero. As seen in Figure (3-7) the output voltage is desired to be a decreasing linear function of load. Implementation of this feature allows the load to be shared equally by two buck choppers running in parallel. The slope of the proposed house curve was 1volt/10% power. Thus, the low load voltage was to set to 305 volts and decreases to a value of 296 volts for a full load.

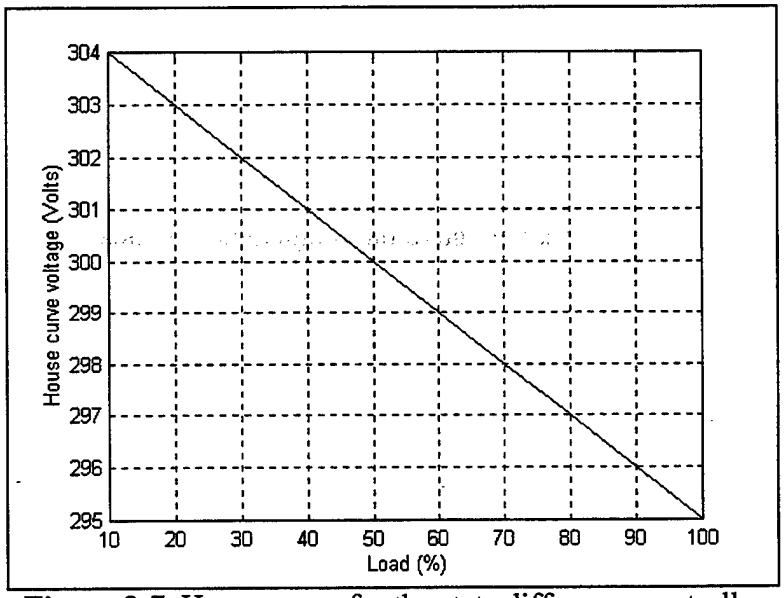


Figure 3-7, House curve for the state difference controller

The specific control law implemented with a voltage house curve is:

$$d(t) = D_{ss} - \left(h_v + h_n \int dt\right)\left[v_c - v_{ref} + \frac{i_o}{10}\right] - h_i\left(i_L - i_o\right) \qquad (3\text{-}37)$$

where

d(t) = time-varying duty cycle
Dss= v_{ref}/E (steady-state duty cycle)
h_v = voltage gain
h_n = integrator gain
h_i = current gain
vc = output voltage
v_{ref} = reference voltage
i_o = load current
i_L = inductor current
E= input voltage

The small-signal portion of Equation (3-37) is:

$$\hat{d} = -\left(h_v + h_n \int dt\right)\left[v_c - v_{ref} + \frac{i_o}{10}\right] - h_i\left(i_L - i_o\right) \qquad (3\text{-}38)$$

The derivative of the small-signal cycle is found from Equation (3-38)

$$\frac{\partial \hat{d}}{\partial t} = -h_i \frac{\partial \hat{i}_L}{\partial t} + h_v \frac{\partial \hat{v}_c}{\partial t} + h_n \hat{v}_c \qquad (3\text{-}39)$$

Substituting Equation (3-20)and Equation (3-21) into Equation (3-39) yields:

$$\frac{\partial \hat{d}}{\partial t} = \left(\frac{-h_i}{L} + \frac{h_v}{RC} - h_n\right)\hat{V}_c - \frac{h_v i_L}{C} - \frac{h_i E}{L}\hat{d} \qquad (3\text{-}40)$$

The formation of the A matrix is similar to that of Equation (3-32) except that the additional state $\hat{d}$ is added and the matrix and becomes:

$$A = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{E}{L} \\ \frac{1}{C} & -\frac{1}{RC} & 0 \\ -\frac{h_v}{C} & \left(\frac{h_v}{RC} - \frac{h_i}{L} - h_n\right) & -h_i\frac{E}{L} \end{bmatrix} \qquad (3\text{-}41)$$

From the A matrix, the characteristic equation is determined to be:

$$s^3 - (\frac{1}{RC} + \frac{h_i E}{L})s^2 + \frac{1}{LC}\left(\frac{h_i E}{R} + E h_v + 1\right)s + \frac{h_n E}{LC} = 0 \qquad (3\text{-}42)$$

The process for determining the required gains for obtaining specific pole placement is based on the coefficients of this characteristic equation. The second and fourth coefficients will reveal the required gain of h_i and h_n directly. The third coefficient will yield h_v after h_i has already been determined. The gains were selected to place the system poles to provide a high degree of damping, quick transient response, no overshoot and far enough away from the switching frequency of 17 kHz so as to avoid interaction between the two. The multiloop model used for simulation has the system poles placed at [-351, -3836,-8] (Hz). The pole selection is consistent with the earlier discussion. The gains were calculated at a minimum load of 100 Ω. As the load resistance decreases the poles tend to migrate from the real axis. Computing the gains at the minimum load ensures that the poles will be sufficiently damped for all values of loads. The gains h_i, h_v and h_n were determined to be:

$$h_i = 0.05 \qquad (3\text{-}43)$$

$$h_v = 0.20$$

$$h_n = 1.0$$

In addition, feed-forward was incorporated to decouple the input from the output and provide quick response to fluctuations in source voltage. The overall state difference control algorithm offers a significant improvement in transient response when compared

to a simple feed-forward, multiloop or integrator-based designs. Figure (3-8) is the closed-loop state-space averaged model depicted in a Simulink simulation diagram. A clock and gain function were used to emulate the startup feature of the controller by ramping the reference voltage. At the end of the startup phase, the reference voltage reaches a constant value.

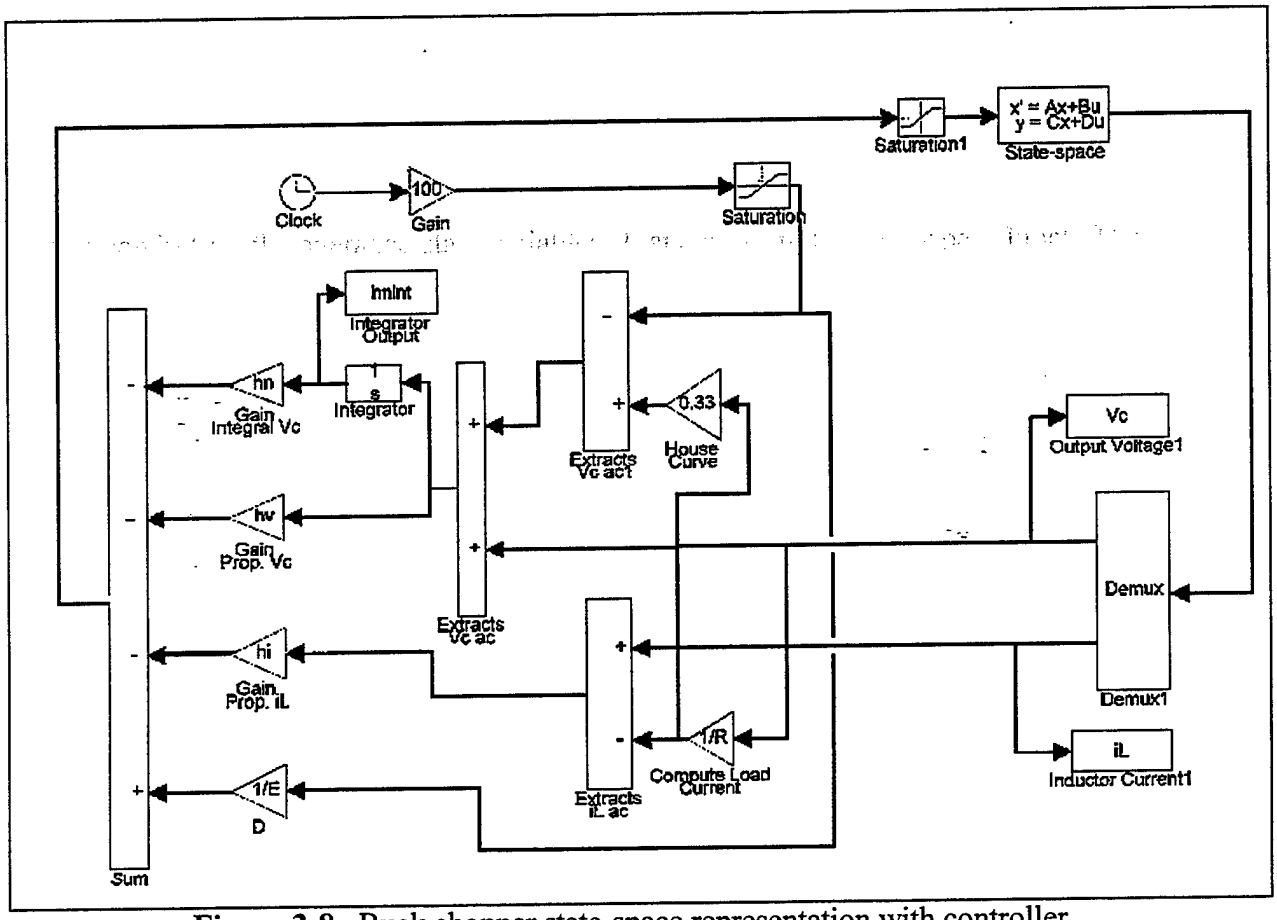
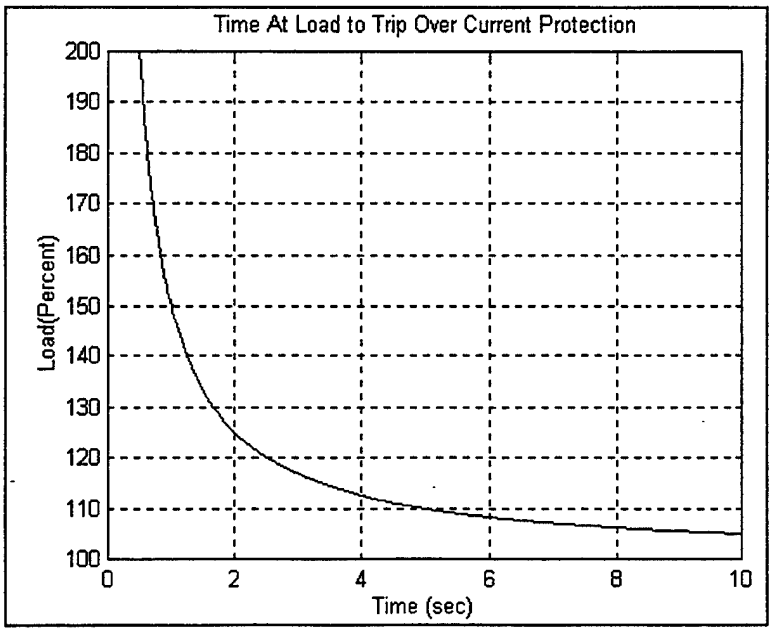


Figure 3-8, Buck chopper state-space representation with controller

B. PROTECTIVE FEATURES

An important benefit of any control scheme is the inclusion of protective features that cause the controller to shutdown or interrupt operations in order to prevent damage to the buck chopper or control boards. The component most likely to fail is the IGBT which

generally fail form excessive junction temperature caused by over current. To prevent switch failure, the control circuit incorporates a thermal shutdown feature that is set below the 150 degree Celsius maximum junction temperature limit recommended by the manufacturer. A thermocouple with a specified set point of 70 °C is mounted on the heat sink close to the IGBT. This form of shutdown requires a reset signal in order to restart the converter. The second form of switch protection is pulse-by-pulse current limiting. The inductor current is monitored by the PWM chip during each cycle. If the current during a cycle exceeds 70A, the IGBT is turned 'off' for the remainder of that cycle. Pulse-by pulse limiting does not require a user reset. The third type of protection is over-current time-out. This protection occurs when the load exceeds 100% and prevents the converter from running an overload condition for an excessive amount of time. This protection's trip point is variable, depending ton the percent load and is plotted below in Figure (3-9).



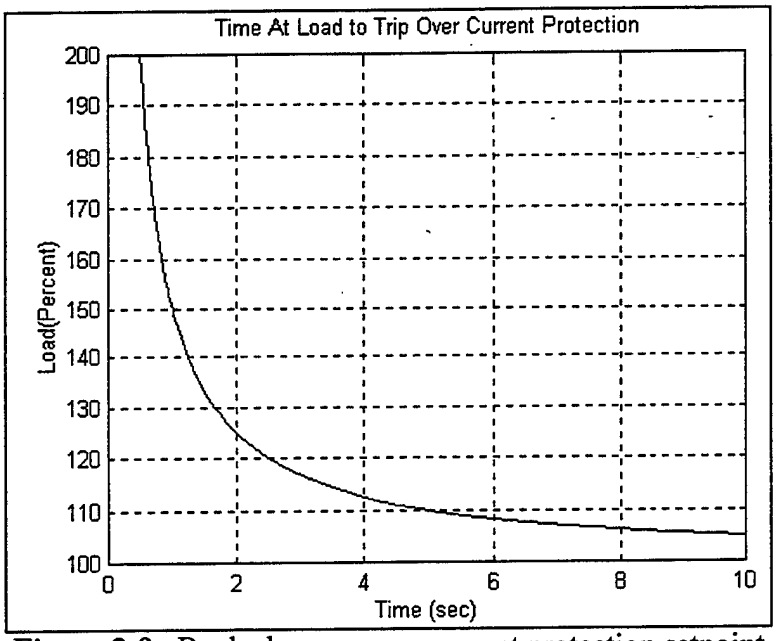


Figure 3-9, Buck chopper over-current protection setpoint

The next area to be explored is simulation of a state difference controller. The model used is developed in the next chapter and several control scenarios are presented.

IV. COMPUTER SIMULATION

A. OVERVIEW

The criteria for evaluating performance of the buck chopper are:

- Startup transient
- Load step change
- Input voltage perturbation
- Reevaluations of the above bullets with 2 converters in parallel

These studies are investigated by developing and implementing a digital simulation model. Since the Power Systems Laboratory power is 'soft', the model will also include source voltage droop. The simulation environment selected for modeling the closed-loop feedback with feed-forward control was the Matlab™ high performance numeric computation and visualization software. The software extension Simulink™ allows quick and simplified simulation of systems which are modeled as objects in a graphic environment[12].

The system models are implemented in two distinct levels. The highest of the levels is the interface of Simulink. At this level, the objects that represent system components are connected with lines which represent the signal paths between specific components. These components may be obtained from the Simulink library or created by the user if the library model is not sufficient. Once the required variables are initialized, the simulation can be started from the Simulink Window (Figure (4-1)). The second level

of the model is Matlab itself. This level uses the variables as initialized and records the data in arrays for plotting. In addition, commands are issued at the Matlab command level to force the change of variables during the simulations and plotting of the data. Such commands include an m-file and the assignment of a new value to a variable. The m-file is a script of Matlab commands that execute each time the script is called by name.

Simulink models are simulated through the integration of a set of ordinary differential equations[12.]. The fifth-order Runge-Kutta method was selected as the algorithm to numerically integrate this set of equations. This method works well with mixed continuous and discontinuous systems. The accuracy of the method is based on a preselected minimum step size in time. Though minimizing the number of steps

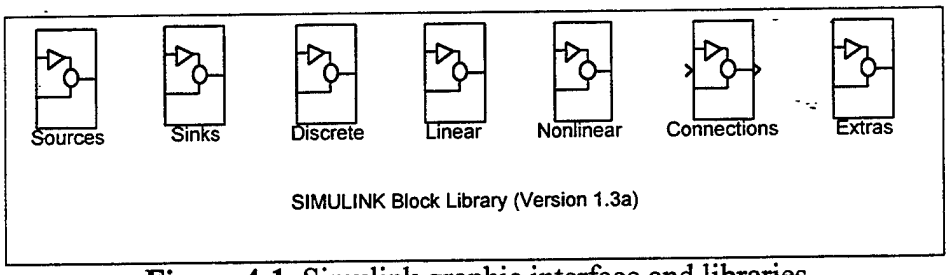


Figure 4-1, Simulink graphic interface and libraries

will accelerate the computation time for a specified simulation time interval, the error may prove to be unacceptable and a shorter step size will be required. This in turn will require more computations and more memory. Based on the time constants anticipated for the buck chopper and control, the minimum time size selected for simulations was two microseconds.

The state-space equations were developed assuming a resistive load. Since the power section of the buck contains a 2-pole output filter, the state-space model will

contain an LRC network. Additionally, the 2-pole low-pass input prefilter was modeled and placed in the signal path of the input voltage to the IGBT. From Equation (3-43), the startup of the circuit is achieved by the linear rise in reference voltage. As reference voltage rises, the steady-state duty cycle term, Dss, rises accordingly. Optimum gain values were determined in Equation (3-43). The simplified Simulink schematic of the controller is shown in Figure (4-2).

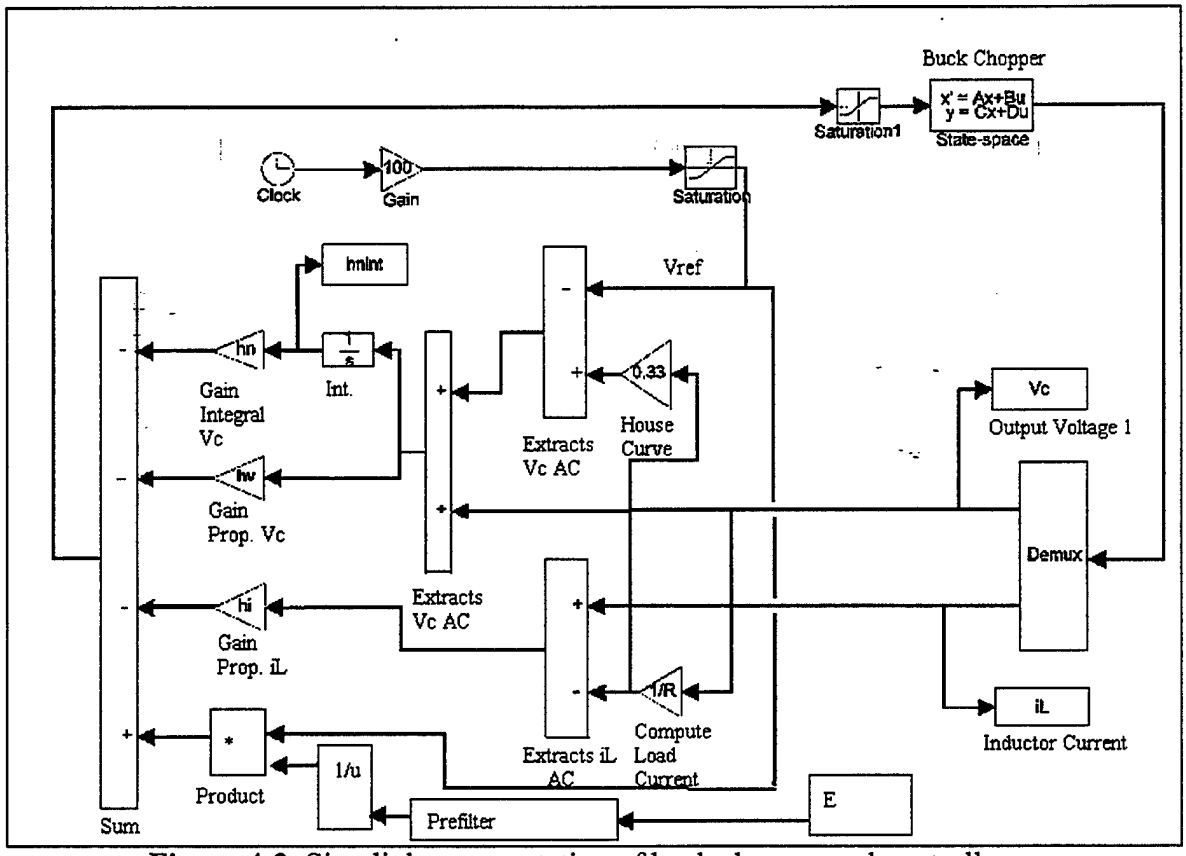


Figure 4-2, Simulink representation of buck chopper and controller

B. CONTROLLER MODEL

1. Buck Chopper Startup

As shown in Figure(4-2), the basic controller model developed for the Simulink environment uses state-space Equation (3-14) to represent the buck chopper. The control algorithm produces the duty cycle and feeds this signal to the representation of the buck chopper. The state-space representation utilizes this variable and produces the averaged output voltage v_c and averaged inductor current i_L. The Demux block in Figure (4-2) acts as a conduit for the averaged state variables i_L and v_c from the state-space block. The load is assumed to be purely resistive and thus the load current is computed from v_c and the load resistance. The difference between load current and inductor current multiplied by *hi* form the current gain portion of the small-signal portion of the control Equation (3-37). The state variable v_c is used for proportional and integral voltage feedback where *hv* and *hn* are the gains, respectively. A proportional load current term is incorporated in the voltage loop to cause droop of the output voltage as load increases. This droop, called a 'House Curve', will allow paralleling of two or more matched converters. The feedback gains *hi, hv,* and *hn* are used to manipulate the poles of the combined converter and controller to provide a stable system and rapid dynamic response.

Startup of the circuit is simulated by a linearly ramping V_{ref} causing the steady-state duty cycle Dss to slowly increase to a preset value. When V_{ref} reaches its low load value of 305 volts, it remains constant. The ramp rate of 100 Volts/sec was selected to limit the peak input current ensure proper switch protection during startup. During this 3

second startup time, 90 Joules of energy must be placed on the output capacitor to charge it to 300 volts. If two converters are paralleled and only one is started, 180 Joules of energy must be supplied by the one converter , doubling the peak startup current.

Figure (4-3) shows i_L, d and v_c as a function of time during startup. The variable d, a direct function of Dss, is shown to steadily increase as the reference voltage rises. The average inductor current i_L , is shown to rise. As discussed in Chapter III, the elimination of overshoot is necessary to prevent load from shifting from one buck chopper to the other during startup of the second.

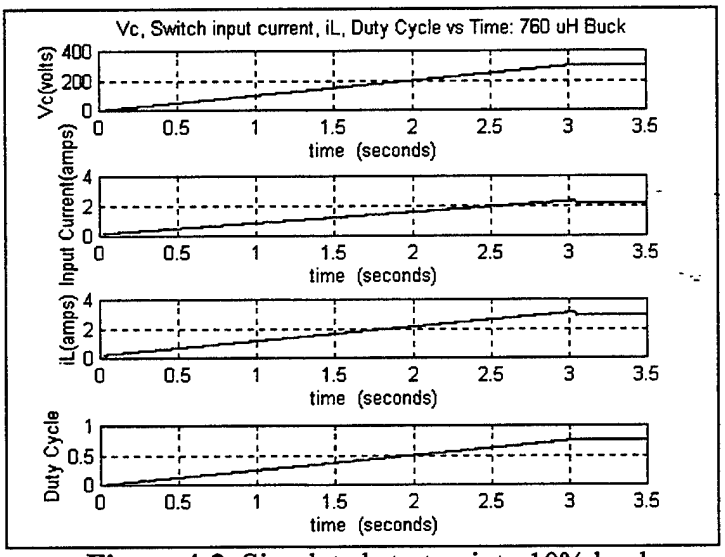


Figure 4-3, Simulated startup into 10% load

To ensure that no protective feature will be triggered during a startup into full load, the ramp simulation was repeated again, this time using a 10 Ω resistor as the load. The results are provided in Figure (4-4).

Figure (4-4) illustrates that the average inductor current does not approach the over-current protection set point of 67.5 amperes. To compute the peak inductor current,

ΔiL was determined from Equation (2-11) to be 5 amps By applying this value with the maximum average inductor current, the maximum peak current is determined in Equation (4-1):

$$iL_{max}(t) = iLavg + \frac{\Delta IL}{2} = 30A + 2.5A = 32.5A \qquad (4\text{-}1)$$

This feature will allow the operator to start the first buck chopper into any load between 10% and 100% without any operating restrictions. Furthermore, Figures (4-3) and (4-4) show that the programmed start of 3 seconds is, in fact, independent of load.

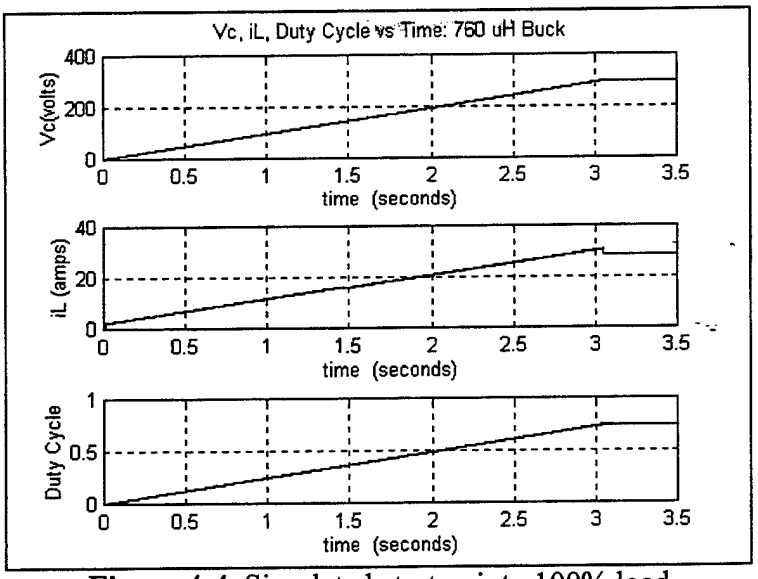


Figure 4-4, Simulated startup into 100% load

2. Source Voltage Sinusoidal Variation

The next phase of simulation explores the effects of source ripple on the output voltage and duty cycle during low-power and high-power operation . This simulation is intended to show that the prefilter component sizing is sufficient to reject the input ripple associated with the rectification of three-phase 60 Hz power. When three-phase 60 Hz

power is rectified in a full wave rectifier, the AC component of the output will have a 360 Hz frequency. This simulation was performed to ensure that source voltage ripple does not induce output voltage ripple via the feed-forward mechanism of the control scheme.

In order to model the rectifier ripple, the source voltage was modeled as the summation of two parts. The first part is a DC value that is held constant with time. The second component is a 4% AC (16 volts Peak-to peak) ripple [2] which represents the maximum theoretical expected ripple without a rectification filter bank. These two components are then added and filtered through the prefilter in order to model the switch source voltage. The simulations of the controller response during high-power operation(Figure(4-5)) and low-power operation (Figure4-6)) show negligible output voltage ripple. Using the maximum of 16 volts ripple, the prefilter does not eliminate all of the ripple, but reduces it to the point that it has no visible effect on the chopper output voltage.

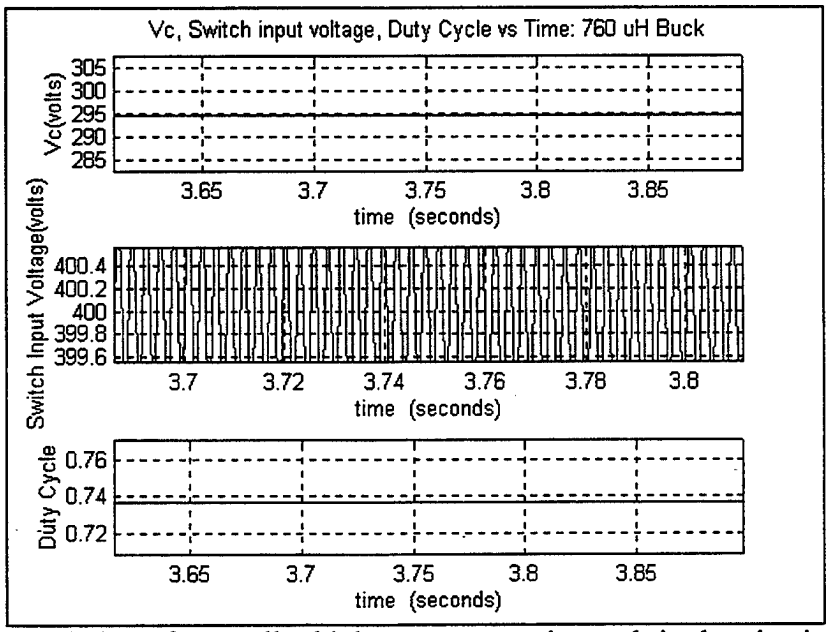


Figure 4-5, Simulation of controller high-power operation and ripple rejection

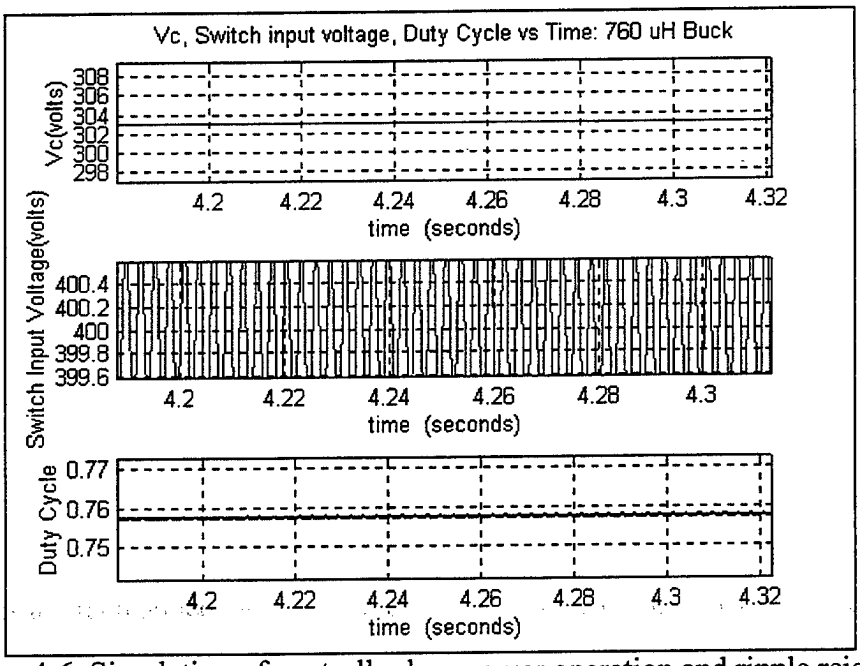


Figure 4-6, Simulation of controller low-power operation and ripple rejection

As seen in the simulation results at high power, the prefilter and controller demonstrate exceptional ripple rejection even when modeled at the maximum theoretical expected ripple. Thus the basic model matches the theoretical result nicely.

3. Step Change in Source Voltage

To determine whether the controller and chopper can respond to typical commercial power events, the next phase of simulation seeks to consider a step change in source voltage. Such step changes are common to both shipboard and commercial electrical distribution systems. The feed-forward loop of the controller was specifically added to force the controller to react rapidly to this type of transient.

In order to mimic this phenomena, the aforementioned DC value of the switch input voltage is divided into two parts. One part will represent the constant value of the

switch voltage while the other portion will be introduced as a step function. A 10% voltage change will be introduced and the transient responses explored. As stated in Chapter III, the mechanism of feed-forward should provide immediate response to the change in switch voltage. This is because the constant steady-state duty cycle is inversely proportional to switch input voltage per Equation (3-35). The prefilter will also act to slow down the rate of change of the input voltage and provide some buffering for the feed-forward loop. The integral feedback will drive the error to zero and the output voltage of the chopper circuit will return to its original value. The results of the simulation are contained in Figure (4-7):

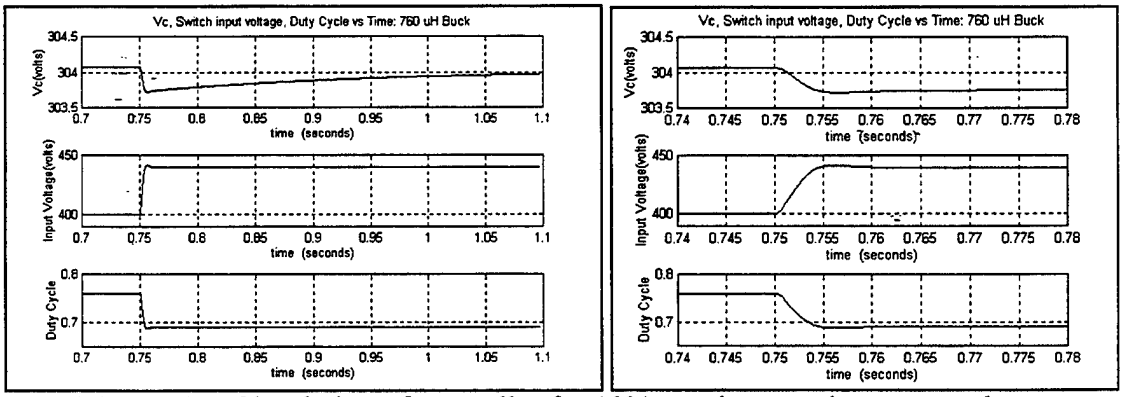


Figure 4-7, Simulation of controller for 10% step increase in source voltage

As can be seen from Figure (4-7), the output voltage of the chopper initially drops approximately -250 millivolts, but recovers within 200 milliseconds to the original output voltage. The rate of recovery from this step change in source voltage is a function of the integral gain. Since the value of the depression (0.08%) is insignificant, the performance of the chopper to a step input change is excellent.

Next, a negative step decrease in source voltage was investigated. As expected, the feed-forward mechanism quickly responds to the change in source voltage while the integral portion of the controller works to drive the final voltage back to the original value as can be seen in Figure (4-8).

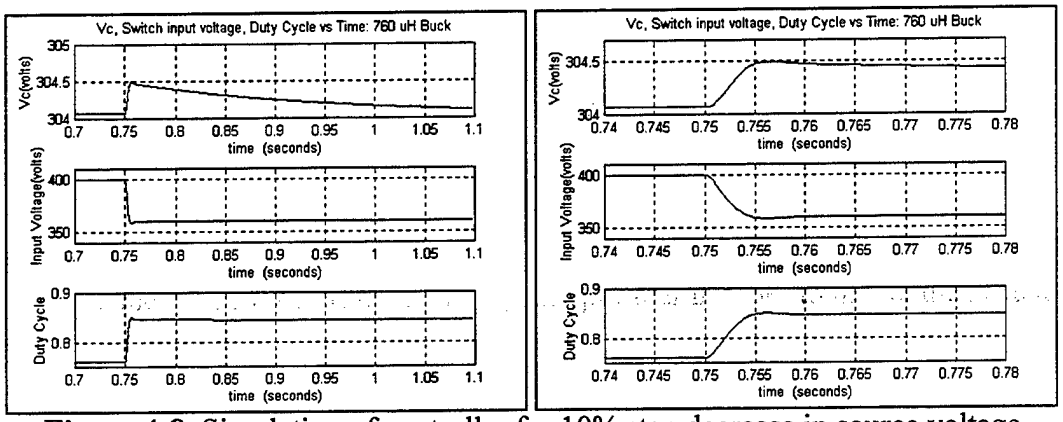


Figure 4-8, Simulation of controller for 10% step decrease in source voltage

Figure (4-8) illustrates the speed at which the controller manipulates the duty cycle and drives the output voltage back to its the original value. Because of feed-forward action, a 10% step change in input voltage causes a 0.13% deviation in the output voltage. Figure (4-9) shows the effect of the control mechanism without the feed-forward loop. The change in input voltage causes a large perturbation in the output voltage and would make the buck chopper unsuitable for the desired application. Furthermore, the large perturbation causes the controller to lower its duty cycle to zero, then raises it back to 1.

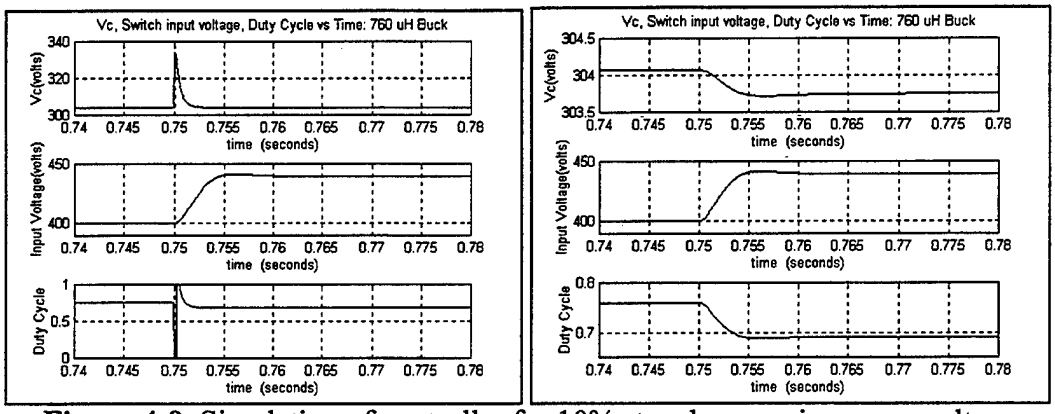


Figure 4-9, Simulation of controller for 10% step decrease in source voltage Left (Without feed-forward) Right (With feed-forward)

4. Source Voltage Droop

Source voltage droop refers to the decrease in source voltage as source current increases. Thus, as more load is added to the chopper, the source voltage decreases. This in turn causes a higher nominal duty cycle which reduces transient 'head-room'.

In order to simulate the line droop, the source voltage is once again separated into two parts; however, the line droop is first computed as a function of load current and then multiplied by a scaling factor in order to mimic the observed laboratory voltage droop. Testing of the buck chopper in the open-loop configurations showed that laboratory source voltage drooped approximately 3 volts per amp. A combination of the load current with a rate limiter are used to model source droop.

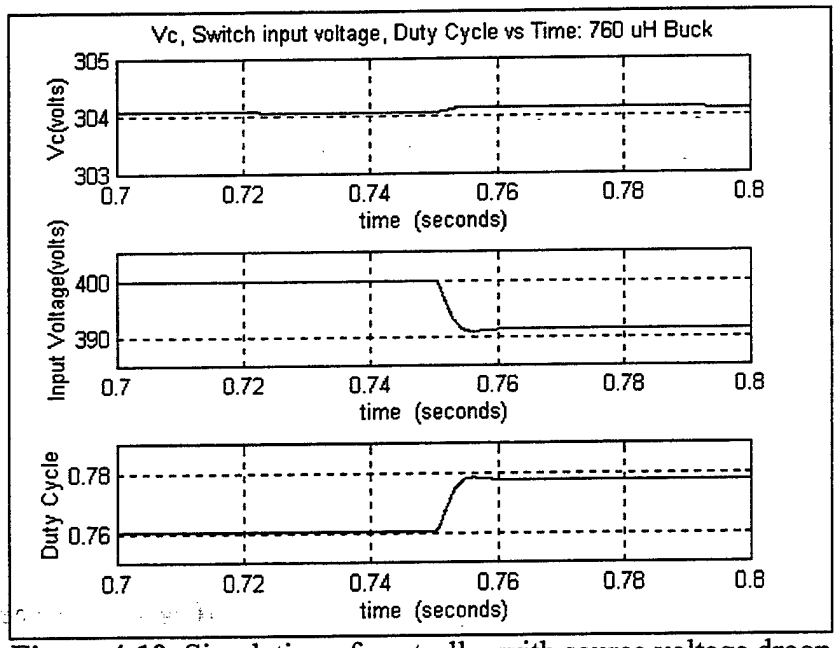


Figure 4-10, Simulation of controller with source voltage droop

Figure (4-10) clearly shows the effects of modeling the voltage droop on the switch input voltage. Even though this is a small load, 3 A of current lowered the switch input voltage by 9 V. A consequence of the droop is that large loads cause even more voltage droop and will cause the controller to increase the duty cycle, decreasing the dynamic range of the control action. This loss of duty cycle 'head room' will cause poor transient response when an increase in load is demanded.

5. Load Transient Analysis

Crucial to the proper operation of a buck chopper is its ability to respond rapidly to transient load changes with minimal fluctuation in the output voltage. To model a load transient three separate concatenated simulations were conducted. The concatenated simulations switch from 10% to 100% and back to 10% load. The simulation concatenation was necessary due to limitations in Simulink which do not allow on-the-fly

parameter changes inside the state-space block. Each concurrent simulation uses the final values of the parameters of the previous run as initial conditions.

Figure (4-11) illustrates the rapid output voltage response for a simulated step increase in load from 10% power to 100% power then back down to 10% power. In order to isolate and document the effects of source voltage droop, the first study does not model the effect.

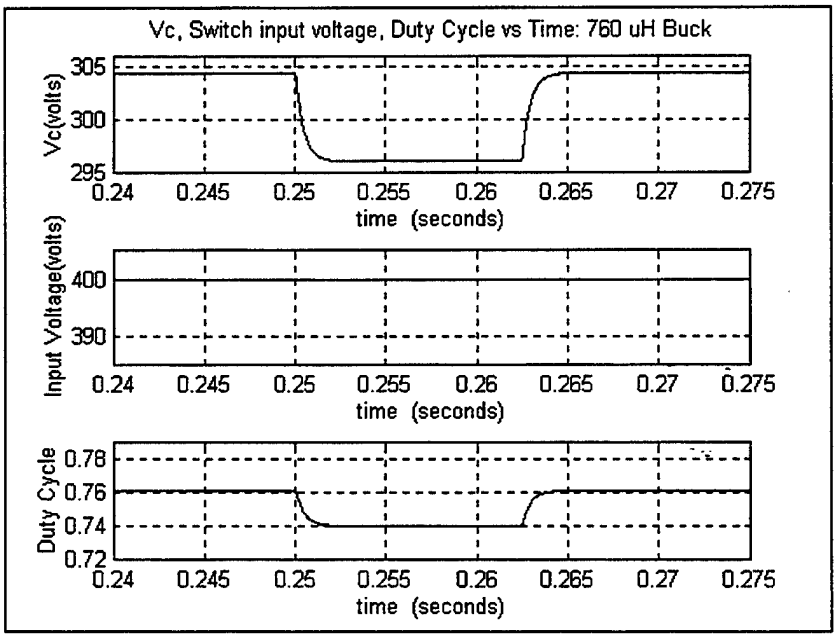


Figure 4-11, Step load change (without droop)

The controller responds rapidly to the load changes. Due to house curve implementation, the duty cycle at high power is lower than the duty cycle at low power. The controller shows fairly good response time with an approximate rise time of 1.25 milliseconds and the transient does not exhibit any overshoot.

With the source voltage droop inserted into the model, the previously described load changes are reevaluated. Figure (4-12) shows quick controller response, the effects

of source voltage droop on the duty cycle and the house curve effect on the output voltage.

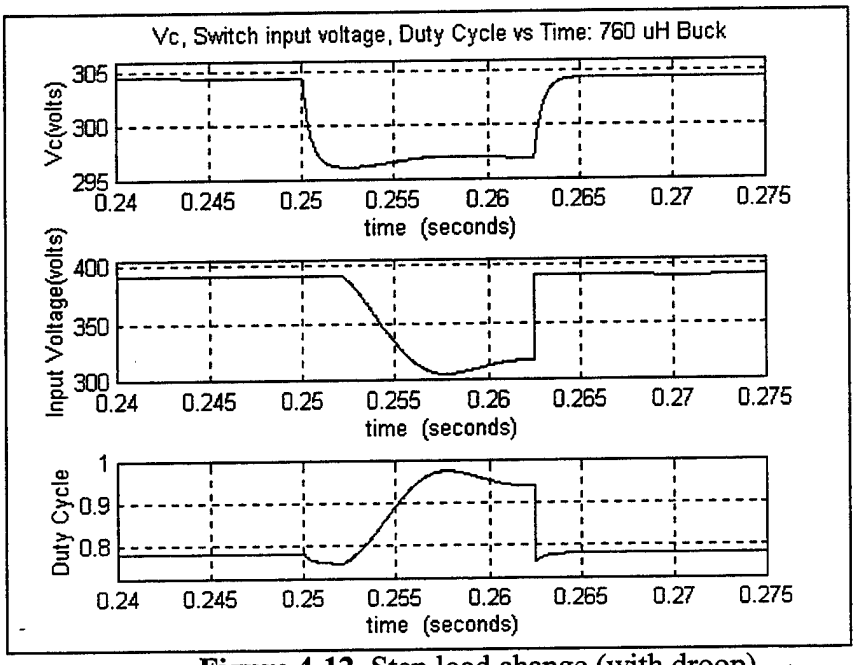


Figure 4-12, Step load change (with droop)

The detailed analysis illustrates rapid voltage response again and shows no overshoot. In this simulation, the rise time is approximately 1 millisecond. The effects of the voltage droop causes the feed-forward portion of the controller to increase the duty cycle. This shows that the presence of source voltage droop decreases controller rise time. The switch input voltage does not decrease as fast as the output voltage due to the presence of the prefilter. The prefilter delays the effect of the voltage droop and allows the controller additional time to respond to the load change. A necessary feature of this controller is that no overshoot may exist, as previously discussed. The duty cycle is seen to continue to increase past the rise time due to the droop of the source voltage.

The original Simulink model shown in Figure (3-8) was modified to Figure (4-13).

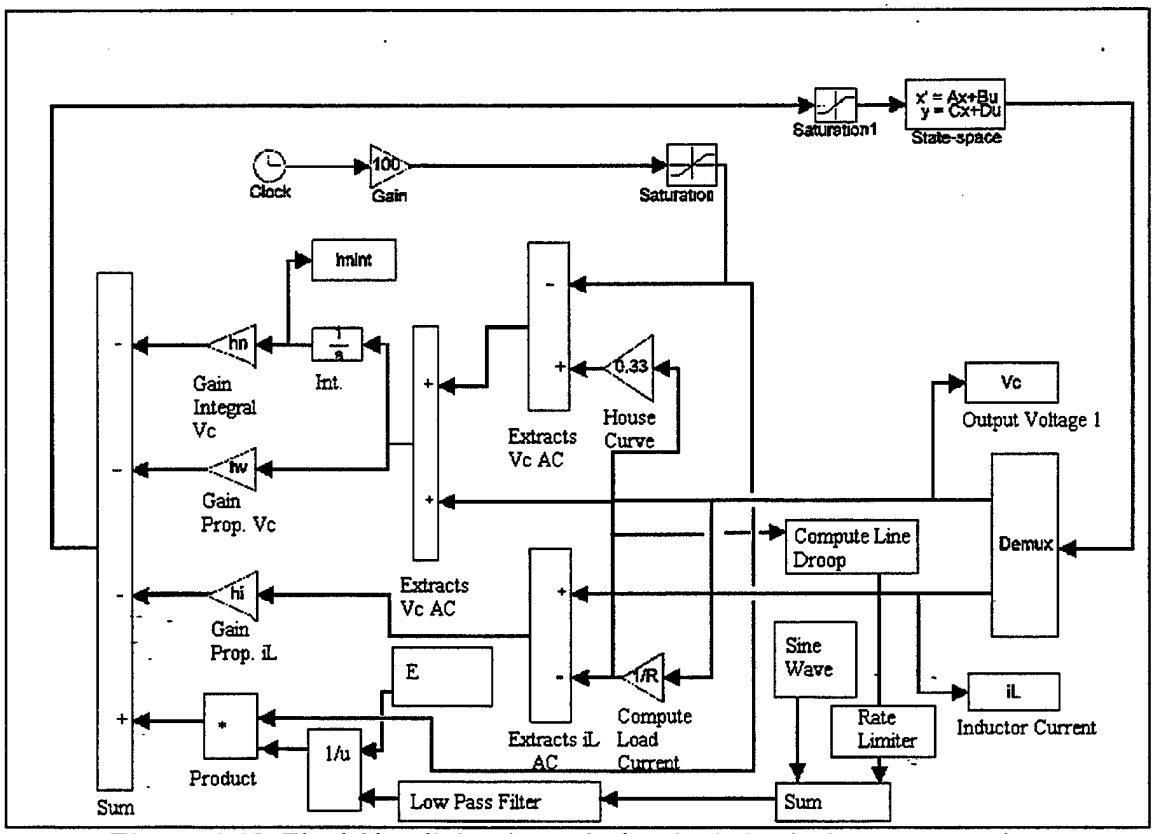


Figure 4-13, Final Simulink schematic for single buck chopper operation

C. PARALLEL OPERATIONS

To simulate the parallel operation of buck choppers, the model developed in the previous section was modified to provide for a limited integrator term as well as to modify the saturation values of the voltage gain. This must be done in order to limit the maximum value and effects on the small-signal portion of the control equation as implemented in the analog controller. These modifications were not required in the previous studies because the small-signal portions of the control equation never exceeded the threshold values implemented in the analog controller. The controller was then

duplicated and the voltage output of the two buck choppers was made common. Each buck chopper was simulated by using the aforementioned state-space equations with the respective component values. Switch input voltage for the two choppers was also made common and thus reduced a significant portion of the required data extraction. Analysis was performed to determine whether a buck chopper could be paralleled with an on-line existing buck chopper by using the previously discussed startup feature of the controller and to determine whether the two choppers would share load. Since both buck choppers were synchronized by the use of a phase-locked loop circuit, the averaged model is a good representation of the actual model. Finally, dynamic analysis was performed to ensure that the paralleled buck choppers could share load evenly in a dynamic load environment. This simulation involved a 50% load step from 4.5 kW to 9.0 kW which was readily available in the laboratory for future use with the prototype unit.

1. Startup of a Second Chopper

To perform analysis on the parallel configuration, the first buck chopper was started and allowed to reach steady-state operation prior to starting the second buck chopper. The results of the startup analysis are provided in Figure (4-14) and show the long-term operation of the second converter coming on-line. As can be seen, the buck machines share load after being placed on line. The duty cycle of the oncoming chopper illustrates that it begins to assume load at 3 seconds after startup. A quick review of the control equation (3-37) shows why the actual assumption of load is delayed. For the oncoming machine controller, the output voltage is already at its steady-state value while

the reference voltage is initially at zero. As a result, the voltage feedback portion of the duty cycle is given by:

$$d(t)_{\text{Voltage gain}} = .2 * (V_{ref} - V_c) = -60 \qquad (4\text{-}2)$$

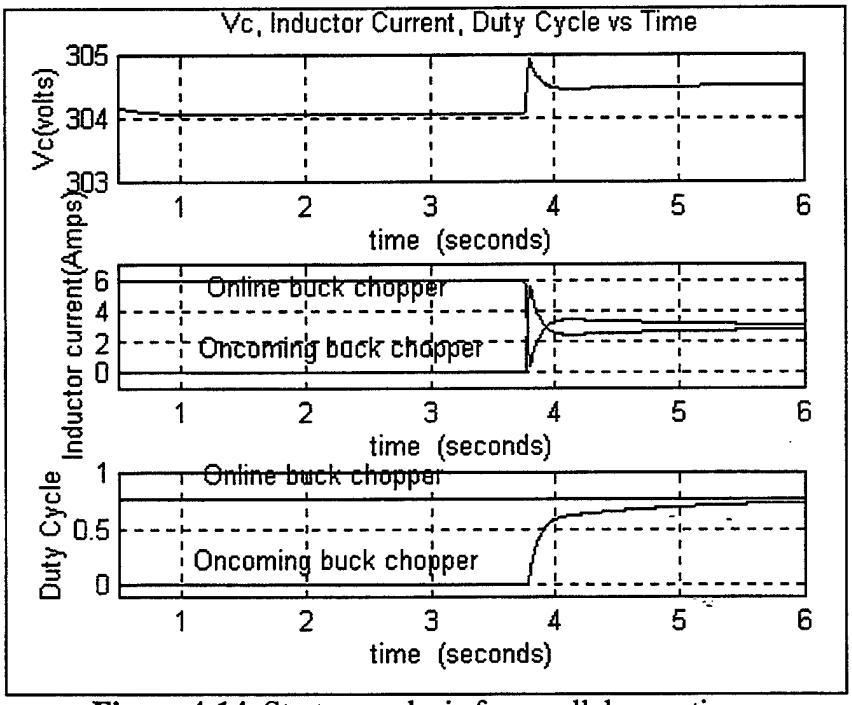


Figure 4-14, Startup analysis for parallel operations

Since the duty cycle is bounded between 0 and 1, the voltage portion of the feedback clamps the duty cycle at zero. This demonstrates why the saturation block was incorporated into voltage feedback portion and a limited integrator placed on the error portion the model. The voltage feedback saturation was set at ±.24 and the integrator was limited at ±.2 based on the prototype analog controller saturation points. With those constraints in place the initial duty cycle created by the summation of the small-signal portion of the control equation is significantly below zero. After the ramping is completed, the reference voltage reaches 160 volts, the feed-forward portion of the small-

signal equation exceeds the summation of the negative small-signal terms and a positive duty cycle can be created. When a positive duty cycle enters into the state-space model, $v_{c(t)}$ and $i_{L(t)}$ start to rise and mitigate the large negative feedback terms. The net effect delays the oncoming chopper from assuming a portion of the load and creates a very nonlinear startup characteristic. This is caused by the fact that Vref has already achieved its terminal value of 305 V before the duty cycle reaches its steady-state value. Despite the high rate of duty cycle increase, the oncoming machine does not produce excessive output voltage and there is no noticeable oscillation in output voltage after the oncoming chopper assumes load. With two machines on-line sharing the same amount of load, the switch input voltage remains at 394 volts and the buck chopper output voltage rises to 304 volts per the 'House Curve'.

2. Dynamic Load Environment

The previously developed model was utilized in a similar manner as outlined in the single buck chopper transient analysis. The loads utilized for the transient analysis mimic a 100% load condition and another that mimics a 50% load condition. As was done in the previous dynamic load testing section, the studies are run consecutively and the results are concatenated for display.

Figure (4-15) shows both buck choppers operating in parallel during a large transient load shift. As was previously discussed in the transient section of single buck chopper operation, the switch voltage undergoes a large step-like increase as load is shed. Output voltage of the buck choppers shows rapid response with a settling time of

approximately 2 ms and no overshoot. Furthermore, the large voltage droop associated with the laboratory power causes the duty cycle to increase to .85 at 100% load. The higher the duty cycle the less available 'head room' exists for transient response. With this margin reduced by the addition of even larger load, the response time of the controller increases. This is because the required duty cycle to achieve a rapid response time would be larger than the maximum bound of 1. As the distance between the steady-state duty cycle and the maximum duty cycle narrows, the response time to an increase in load lengthens.

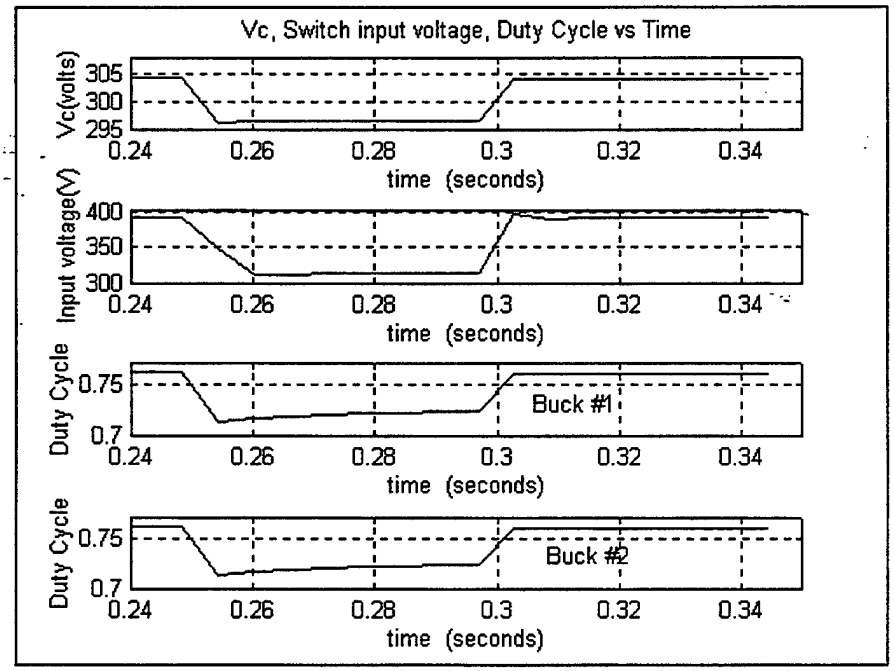


Figure 4-15, Step load change for parallel operations

With the buck chopper model simulation completed and investigated, the next chapter will introduce the prototype development.

V. PROTOTYPE CONTROLLER

The development of the analog controller was designed to implement the state difference equation formulated in Chapter III. In addition to the central control board, a sensor board and phase-locked loop board are also described. The sensor board is used to gather, isolate and scale the control board inputs while the phase-locked loop circuit synchronizes the clock speed of the two separate control boards. The controller is evaluated through a series of tests prior to connecting it to the power section of the buck chopper. These tests are outlined in this chapter. After connecting the controller to the chopper, closed-loop testing is explored and compared to simulation results. Lastly, two buck choppers were load tested in parallel for further model validation. A Netlist with a list of component values and locations for each circuit board is included in Appendix B.

A. CONTROL CIRCUIT DESIGN

The circuit block diagram depicted in Figure (5-1) illustrates the major subsections of the controller in relation to the various parts of the buck chopper. These subsections include a common power supply, a buffer stage, the main control, circuit protection and the pulse width modulator (PWM). The signal derived in the main control section is sent from the PWM to the driver board where it is amplified to drive the IGBT gate.

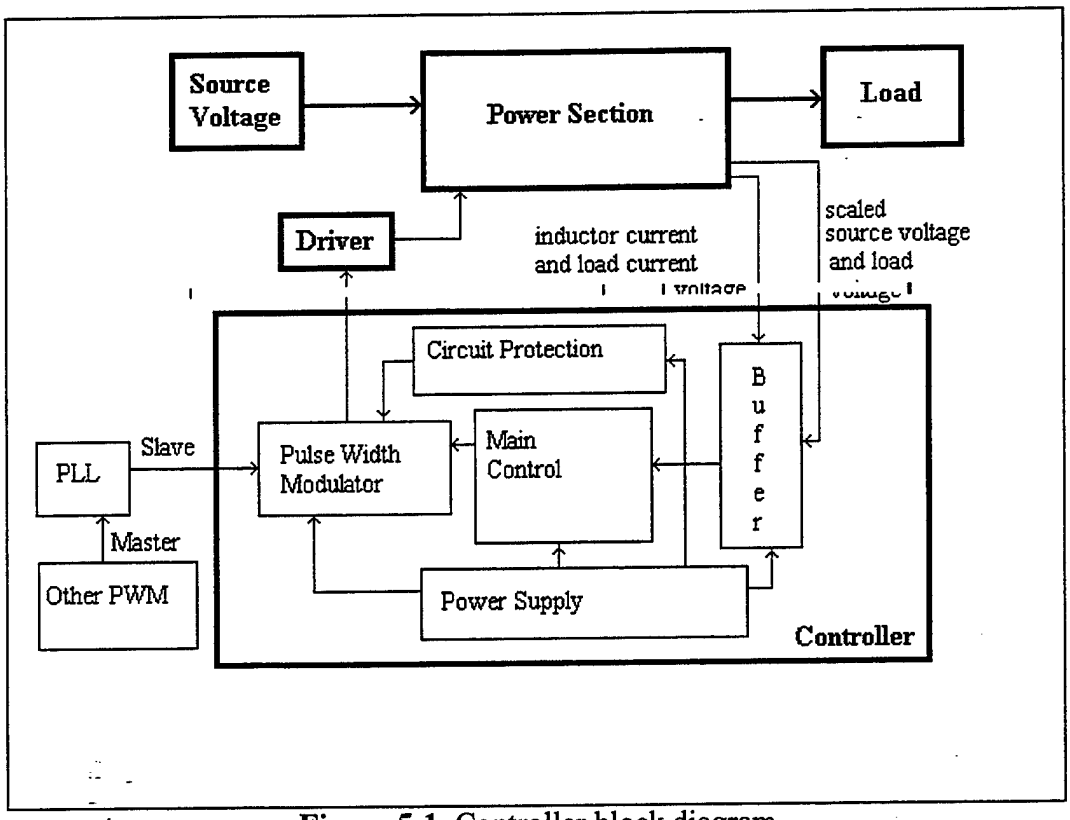


Figure 5-1, Controller block diagram

The operation of the controller subsections is straightforward. Input and output voltage are scaled using precision resistor networks, and the load and inductor current are uncovered through the use of Hall effect sensors. Additional details are documented in a later section. These four scaled signals are fed to a buffer stage to provide high impedance isolation from the measuring devices to the controller. A single op amp circuit establishes a reference voltage which is a scaled version of the desired output voltage. The outputs from the buffers along with reference voltage are fed directly to the main controller for use.

The main control stage implements the algorithm summarized in Equation (3-37) as follows:

$$-(i_L - i_o)h_i - \left(v_c - v_{ref} + \frac{i_o}{10}\right)h_v - \int\left(v_c - v_{ref} + \frac{i_o}{10}\right)h_n \qquad (5\text{-}1)$$

where the currents and voltages from the sensors are scaled by 1/50 and 1/10 respectively. The output of the main control is a 0 to 10V analog signal proportional to the duty cycle. This is sent to the pulse width modulator chip which converts it to a gate drive square wave signal. This driver circuit signal is fed to an optically isolated driver board which is mounted directly on the IGBT. The circuit protection subsection acts to disable the PWM when a circuit protective feature is initiated, or when operator intervention, such as a shutdown, is initiated.

1. Power Supplies

A small isolated switching DC-to DC converter by Datel was used to establish the ± 15 and +5 V for the control board. Isolation is provided by both the Datel and the filament transformer used to power the Datel. Electrical isolation is important in order to prevent circulating ground currents which could cause damage to the equipment and circuit. Figure (5-2) shows the schematic diagram for the power supplies. All integrated circuit supply pins on the controller have 0.1 μF bypass capacitors to ground for transient response and elimination of high-frequency noise on the power busses. A 117 to14 Vct @ 60 Hz transformer, a full wave bridge rectifier and a 2200 μF capacitor for ripple produces an unregulated ± 11VDC. This is sufficient to supply the Datel with its needed input voltage between 9V and 18V.

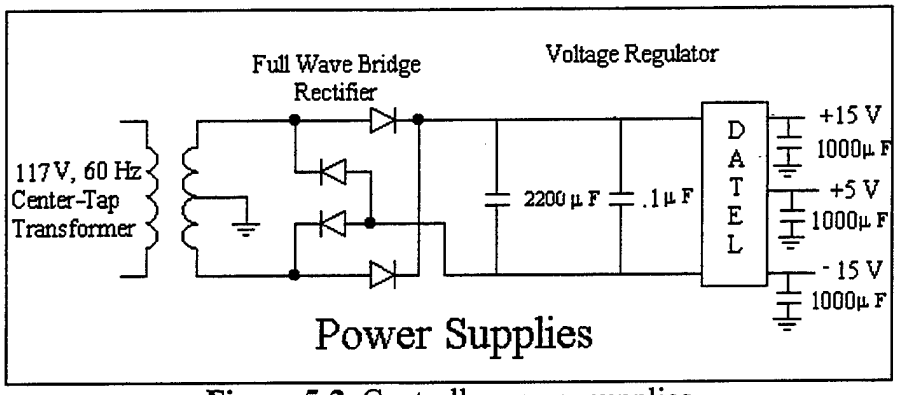


Figure 5-2, Controller power supplies

The DATEL can handle 1 Amp output current on the +5 V output and 200 milliamps on the ±15 V terminals. The 1000µF capacitors on the output of the Datel help reduce switching noise.

2. 25 pin Connector and Buffer Stage

The controller buffer circuit shown in Figure (5-3) is constructed using one LM 342 quad operational amplifier configured for unity gain. The 25 pin connector interfaces the inputs to the buffer stage on the control board. The buffer provides a high input impedance interface for the sensing circuit and a low output impedance for the control circuit.

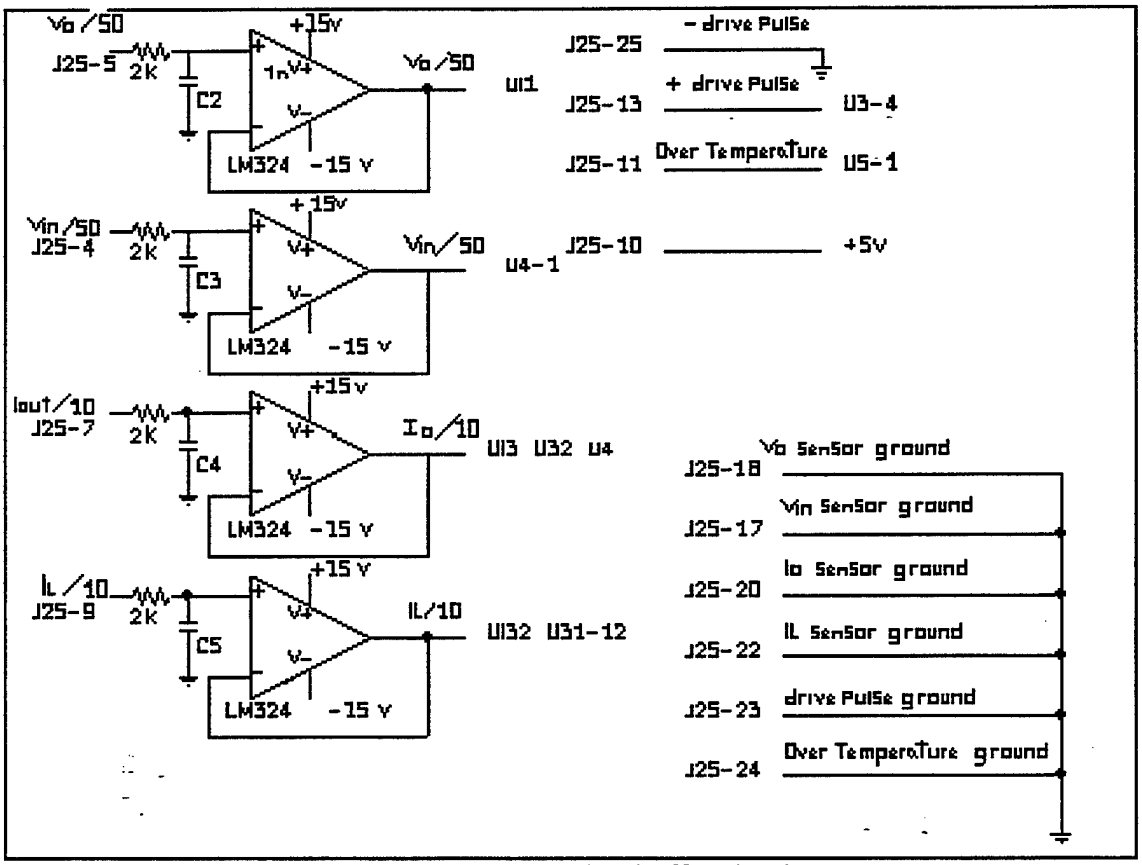


Figure 5-3, Controller buffer circuit

3. Main Control Stage

The main control section excluding protection consists of an LF 347 quad operational amplifier and an AD 534 analog voltage multiplier. As can be seen in Figure (5-4), the main control section utilizes a reference voltage and the four buffered outputs from the sensor board. The AD 534 is configured as a divider and establishes the steady-state duty cycle Dss. Dss is simply the ratio of the reference voltage to the source voltage and provides feed-forward control action. The LF 347 quad operational amplifier is utilized to compute the current difference, (iL-io), compute the voltage error with the

house curve $\left(v_c - v_{ref} + \frac{i_o}{10}\right)$, integrate the voltage error term and sum all the resultant terms. A unity gain differential amplifier establishes the current response term. This is fed to the summing amplifier with a gain of 5. Thus, the small-signal gain for the current feedback can be found using Equation (5-2) where the PWM chip requires a 0 to 10V signal for a 0 to 100% duty cycle.

$$10 * d(t) = \frac{5\left(i_L - i_o\right)}{10} \tag{5-2}$$

This can be simplified to:

$$10 * d(t) = h_i(i_L - i_o) \tag{5-3}$$

where loop gain $h_i = 0.5$.

The voltage error with house curve is produced using a summing amplifier. The voltage terms are set at unity gain while the load current term gain is 1/15. The equation for the error voltage is:

$$V_{error} = \frac{V_{ref} - V_c}{50} - \frac{1}{15}\left(\frac{i_o}{10}\right) \tag{5-4}$$

This signal is simultaneously sent to a limited integrator and the final summing amplifier. The integrator inverts and amplifies the signal by a factor of 100 prior to summing it into the final operational amplifier. The integrator output signal is:

$$V_f = 100 \int V_{error} \tag{5-5}$$

This signal along with the voltage error signal of Equation (5-4) and current difference signal of Equation (5-3) and Dss from the AD 534 are fed to the summing amplifier which is configured for specific input gains as shown in Equation (5-6). The scaled signal is:

$$V_{output} = \left(\frac{V_f}{5} + 10V_{Dss} + V_{error} + \frac{(i_L - i_o)}{2} \right) = 10 * d(t) \qquad (5\text{-}6)$$

The scaled signal is produced in the operational amplifier shown in the upper right section of Figure (5-4). The output of this operational amplifier (Vd(t)) is fed to the pulse width modulator.

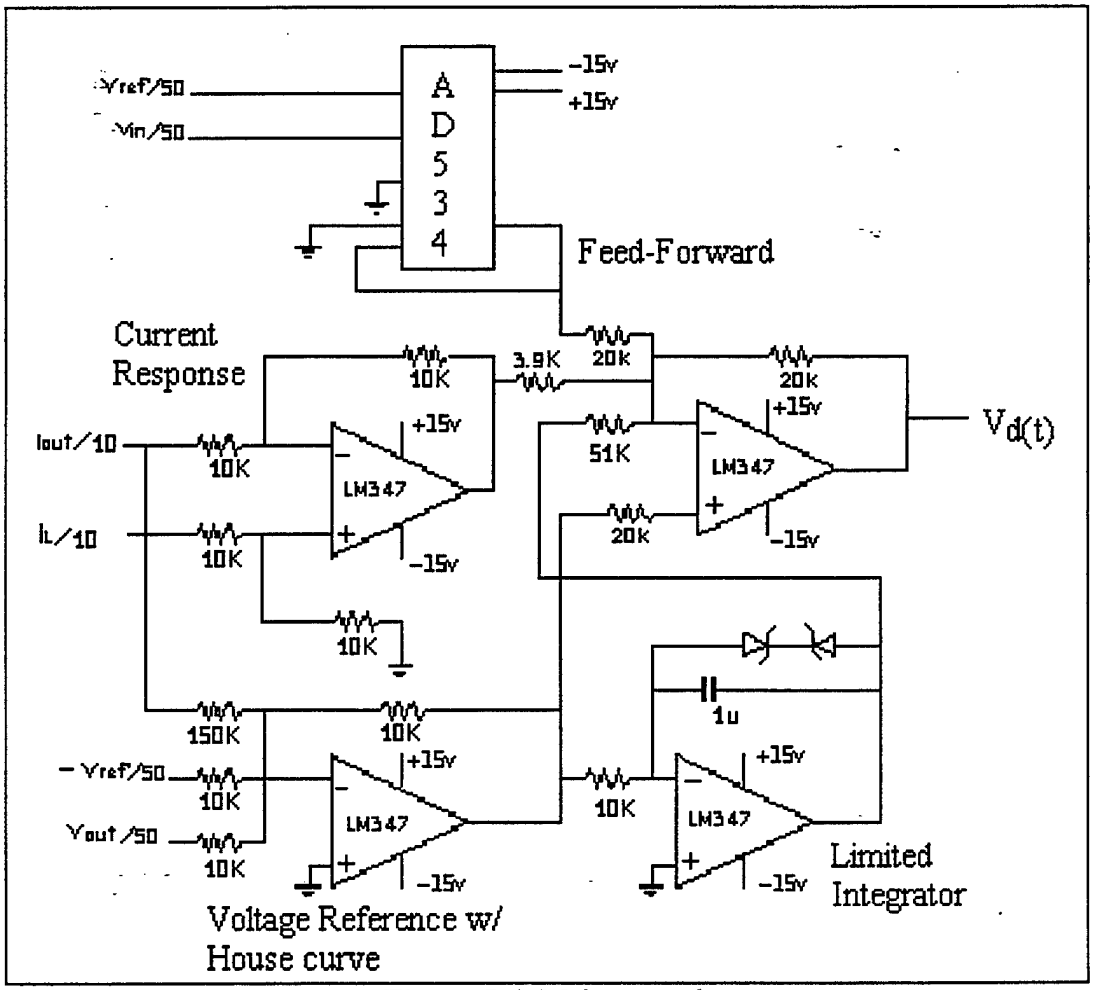


Figure 5-4, Main control

4. PWM Circuit

The other crucial component of the closed-loop feedback with feed-forward control is the pulse width modulator, which is comprised of the UC3637 chip. It receives the analog input signal 10*d(t) from the main control stage and produces a square wave signal for the driver circuit. The duty cycle of the pulses is equal to the input analog signal divided by ten. The output driver signal is fed to a driver board mounted directly on the IGBT. In addition to producing the driver signal, the PWM chip also provides the means for implementing pulse-by-pulse over-current and over-temperature protection. To do this, the protection stage of the controller produces a signal that disables the PWM chip when protection is required . By disabling the PWM stage, no driver signal is sent to the driver-board and the switch is kept open. When the switch is shut, it is no longer subject to over-current damage and will only be subject to over-voltage failure. The PWM is energized by the ± 15 V regulated power and the +5 V reference voltage as shown in Figure (5-5). The +5V reference voltage is used in the over-current protection circuit to be described in the next section.

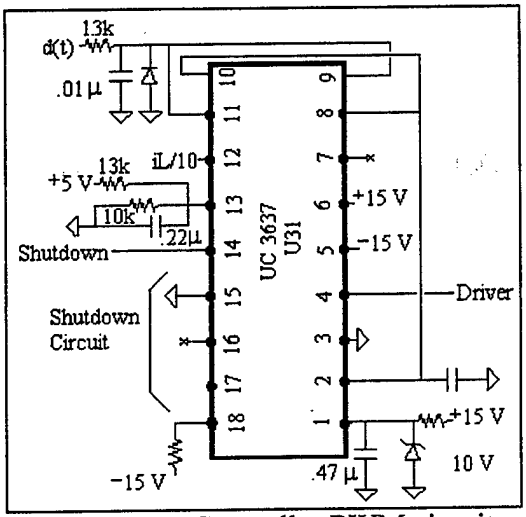


Figure 5-5, Controller-PWM circuit

5. Protection, Startup and Reference Stage

The protection stage of the buck controller is comprised of two circuits. The first includes the pulse-by-pulse feature of the UC3637 chip described in the previous section. This circuit protects the IGBT from exceeding its 90A current rating. If a fault occurs, the inductor current i_L will rise rapidly. If its value exceeds 67.5 A, the signal fed to the comparator located inside the PWM chip will cause the PWM output to go low. With no signal sent to the IGBT driver board, the IGBT will remain open and the only mode of switch failure would be that of an over-voltage condition (See Figure (5-6)).

The second protection circuit is over-current time out. This circuit protects components from thermal damage when i_o exceeds a limit for a prescribed time. For the buck controller, a 150% over-current / 1 second time out was designed. Utilizing the operational amplifier in the UC3637 (pins 15-17), an integrator was designed such that if the scaled signal $i_o/10$ where to exceed 4.5V, the integrator output would reach -10V in 1 second. This voltage causes the comparator U7 output to go high which, in turn, causes OR gate $U5_2$ to go to its high state. When this occurs, the output of OR gate $U5_4$ will go to its high state and send a high voltage to comparator U8. As a result, comparator U8 output toggles high, sending a shutdown signal to pin 14 of the PWM chip.

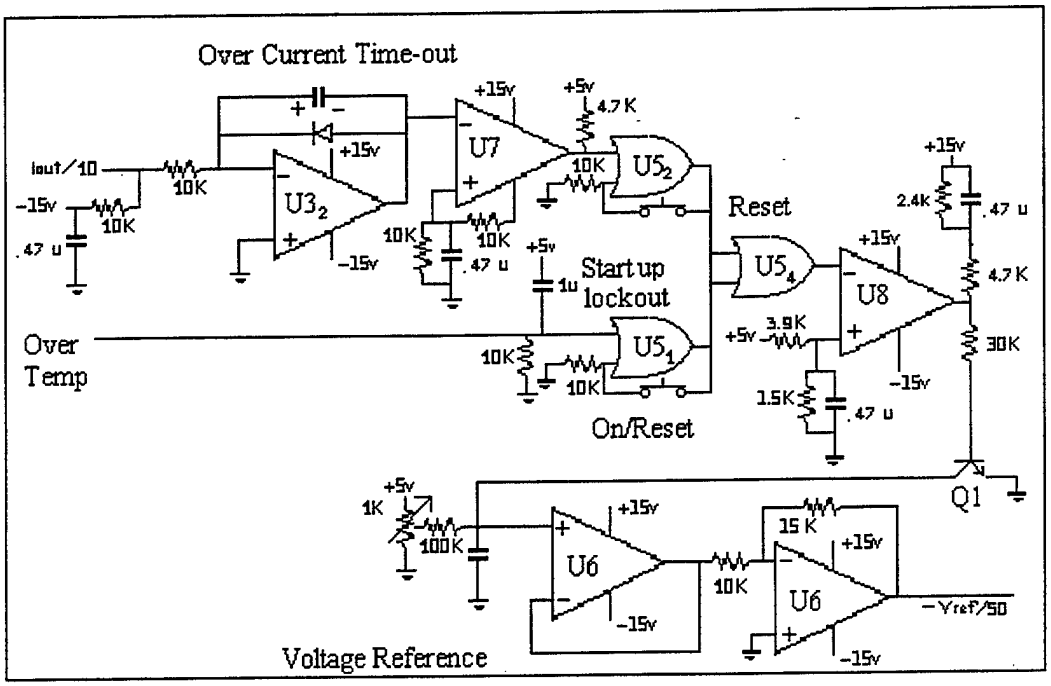


Figure 5-6, Protection, startup and voltage reference circuit

The startup circuitry of the buck controller implements a ramp up of the duty cycle to its steady-state value from zero initial conditions. When the controller is initially energized, OR gate $U5_1$ goes high due to a +5V pulse generated by the RC circuit at input pin 1. As a result, the output of $U5_4$ toggles 'on' which , in turn, causes the output of comparator U8 to go high. With the base of Q1 positively biased, Q1 turns 'on', which causes pin 3 of the voltage follower U6 to go low and prevents a reference signal from being generated. The end result is that a lockout occurs and prevents a duty cycle waveform from being generated "instantaneously". Without such a lock out, an instantaneous change in duty cycle would result in high currents and voltages causing a protective feature to be initiated and the main switch to be shut down. With the initial condition of d(t)=0, the buck chopper is started by ramping up the reference voltage,

which will cause the duty cycle of the switch to ramp up at the same rate. This slow (over a 3.5 sec period) and controlled ramping of the duty cycle ensures that the switch does not experience excessive voltages and currents during the startup phase. By resetting momentary switch labeled On/Reset in Figure (5-6), the OR gate $U5_2$ toggles to an 'off' state. This in turn causes the OR gate $U5_4$ to go to an 'off' state. The comparator output drops to a low state thus removing the positive biasing of Q1, which turns 'off'. As a result the input voltage applied to pin 3 of U6 begins to ramp up through the charging path established by RC (the combination of which produces a time constant of .6 second). Ramping Vref causes d(t) to ramp to its operating value thus preventing large voltage and current oscillations on startup. After startup, the reference voltage continues to be supplied through the MC1458 dual op amp package configured as a voltage follower / inverting op amp pictured as U6 in Figure (5-6).

A manual reset button has been inserted in order to allow the operator to shut down the controller and also allows the resetting of the reference voltage following normal shutdown. This is facilitated by inserting a momentary reset switch into the over-temperature path which feeds the OR gate $U5_2$. Triggering the momentary switch pulses $U5_2$ which causes the output of the OR gate to go to its high state. This output causes the output of the OR gate $U5_4$ to go to its high state and inserts a positive voltage on the positive input to the comparator U8. The comparator U8 output establishes a positive voltage on pin 14 of the PWM circuit which causes the PWM to shutdown.

Figure (5-7) shows a picture of the analog controller and documents the physical location of the components described above. The small potentiometer shown in the upper

center portion of Figure (5-7) corresponds to the adjustable resistor included in the lower section of Figure (5-6). This potentiometer is used to adjust the reference voltage and thus change the output voltage to compensate for any thermal drift that may occur during circuit operation.

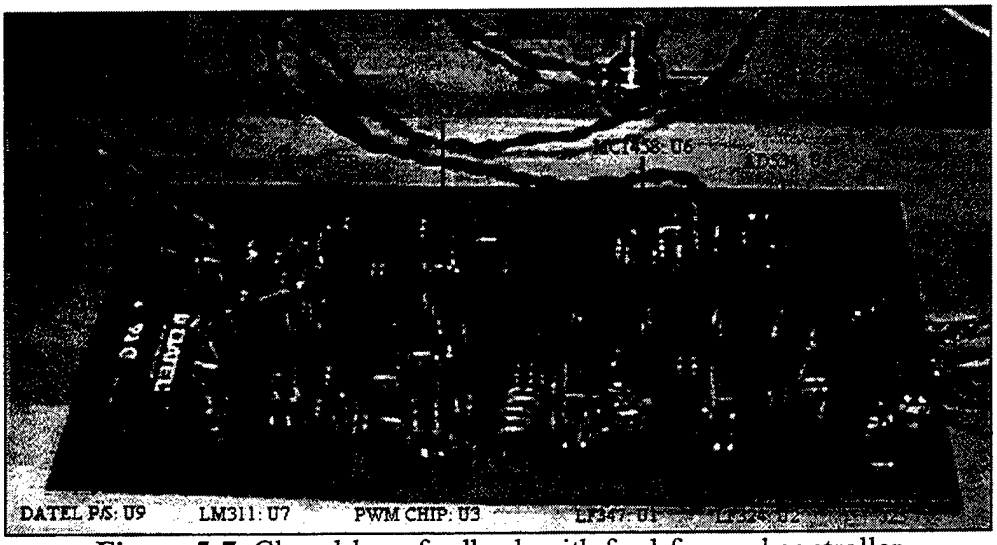


Figure 5-7, Closed-loop feedback with feed-forward controller

B. SENSOR BOARD CIRCUIT DESIGN

The sensor board extracts the input and output voltages and inductor and load current for both buck choppers. Voltages are reduced using a precision resistor network which is then fed into an AD215 voltage isolator. This is necessary to ensure that the buck chopper high voltage is not directly communicated to the controller. The current is detected using two Hall effect current sensors. To avoid impedance mismatches the AD215 voltage sensors and the Hall effect current sensors are fed into the unitary gain buffer stage on the controller.

1. Power Supply Circuit

A common power supply was used to provide power to the AD215 voltage isolators and the Hall effect current sensors. As shown in Figure (5-8), a 117/28 V_{CT}, 60 Hz transformer and full wave bridge rectifier with 2200 μF capacitors for ripple smoothing yields unregulated ± 22 VDC. The unregulated voltage is fed to a set of voltage regulators, the MC7815 and MC7915, producing ±15 V. These three-terminal positive and negative voltage regulators can handle in excess of 1 Amp output current with proper heat sinks.

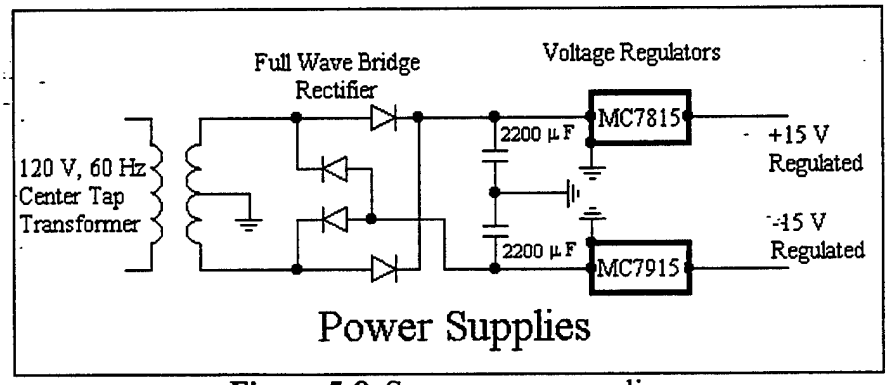


Figure 5-8, Sensor power supplies

2. Voltage Measuring Circuit

The voltage sensing circuit is shown in Figure (5-9). In order to provide electrical isolation to the control circuit, two AD215 voltage isolators are used to measure the buck input and output voltages. The voltage range for the AD215 is ±10 V. The 10V zener diode limits the maximum voltage input to the AD215 in the event that the voltage divider network fails. In addition, a 2 kΩ resistor on the input of the AD215 protects the device from excessive current should the zener fail during a voltage transient. The AD215

was configured for unity gain operation, hence pins 3 and 4 were tied together. The integrator requires a negative input voltage in order to generate the positive output voltage for use in the comparator. In order to achieve an inverted input to the integrator, the inputs to the voltage isolator were inverted. This is much simpler than setting up the voltage isolator circuit in an inverting configuration.

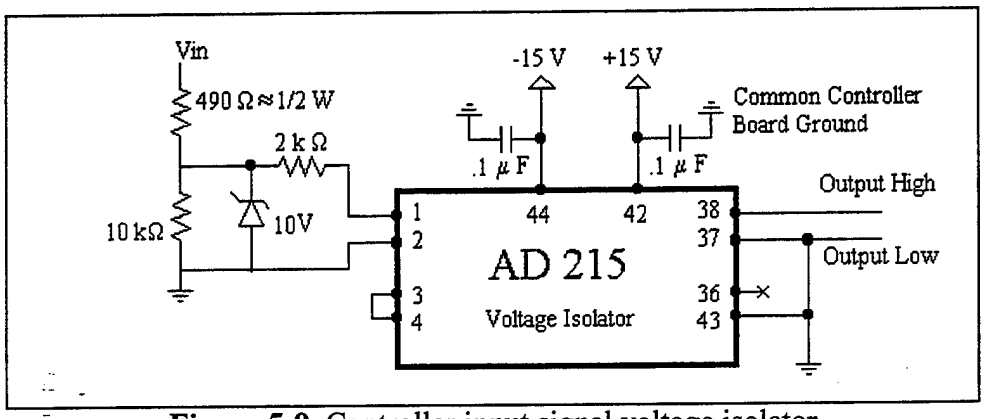


Figure 5-9, Controller input signal voltage isolator

3. Current Sensing Circuit

The inductor current and load current are sensed using two CL-50 Hall effect sensors. The Hall effect sensors provide electrical isolation between the current-carrying conductor and the output of the sensor. As shown in Figure (5-10), the CL-50 requires regulated ±15 VDC and produces a scaled output signal that is one one-thousandth of the RMS value of the current. A 100Ω precision resistor is used to convert the current to a voltage where the voltage produced by the Hall effect is proportional to 1/10 of the current. This voltage is fed to the buffer stage of the control board.

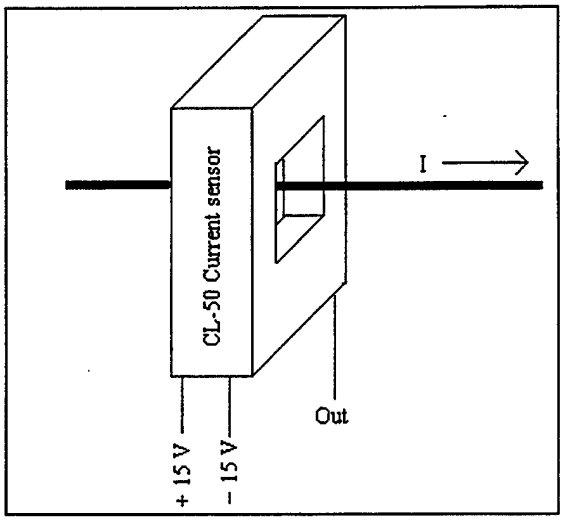


Figure 5-10, Current sensor circuit

C. PHASE-LOCKED LOOP

The phase-locked loop (PLL) circuit, depicted in Figure (5-11), was designed to ensure that both buck choppers operate in synchronization. This is necessary to avoid large circulating currents between the chopper output filters caused by the time variant minor changes in voltages. The phase-locked loop draws power from the $\pm$15 V regulated power located on one of the two control boards. The circuit requires frequency inputs from each controllers PWM chip. These inputs are the oscillator frequency of the PWM chips, where one is designated the master and the other is the slave. The PLL circuit feeds back a signal to the slave PWM chip that causes that PWM to match the phase of the incoming signal. To do this, the master and slave PWM waveforms are fed to two comparators designed to toggle to the high state when the voltage of the input waveform exceeds 9V. The outputs of the comparators are fed to a dual NOR gate R-S flip flop connection. The combined NOR network acts to set the PLL output in the 'on' state when the slave comparator exceeds the setpoint value of 9V and is held in the 'on'

state after the comparator output toggles 'off'. Likewise, the master signal is fed to its comparator, which toggles 'on' when the master input voltage exceeds the threshold value of 9V. The comparator output acts to reset the value of the NOR network. Thus if the slave frequency lags the master frequency, the PLL will be placed in a set condition longer than a reset condition. Since the output of the PLL is fed back to the slave PWM frequency input, such a condition will result in an increase in the slave frequency. In case the slave frequency rises above the master frequency, the NOR network will spend more time in the reset condition than the set condition causing the frequency feedback signal of the PLL to decrease. This in turn causes the slave frequency to decrease.

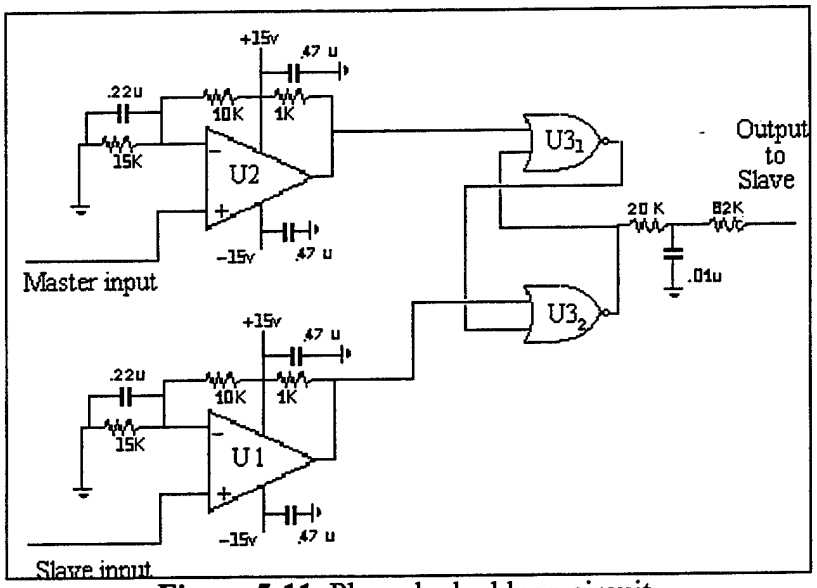


Figure 5-11, Phase-locked loop circuit

D. CONTROLLER BENCH TESTS

The controller was bench tested to ensure proper protective feature operation and output waveform generation prior to connection to the power section. Various inputs were used to inject the necessary signals into the controller to evaluate response. The first

test involved a series of simulated injected values to ensure that the PWM produces a square wave output. The last two tests ensured that the protective features of the controller would be invoked if the proper conditions were met.

1. Output Waveform Verification

The first test conducted is a basic open-loop test to verify that the unit generated a proper output waveform. To implement this, the basic controller was run with a constant scaled source voltage with a jumper installed in the main control section. This jumper was used to close the loop and replaced the buck chopper itself. With the loop closed the summing amplifier produced a small output signal d(t). The resulting duty cycle formed from the voltage gain and current gain terms is fed back to the reference voltage input, thus setting the error signal of the small-signal portion of the control (Equation (3-37)) to zero. The result is a constant duty cycle determined solely by the feed-forward portion of the controller. The controller output waveform is illustrated in Figure (5-12).

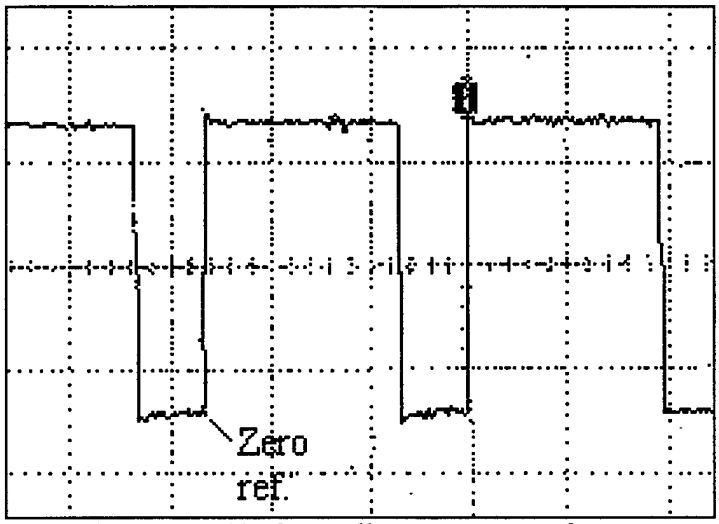


Figure 5-12, Controller output waveform
20 μsec/div. CH1 input to driver signal 5V/div

2. Pulse-by-Pulse Over-Current Protection

The pulse-by-pulse current limit feature of the UC3637 chip was tested to ensure that protection would be initiated for the proper conditions. This would protect the IGBT from exceeding its rated capacity of 90A. If a fault were to occur, then inductor current would rise. When the value of $i_L/10$ exceeds approximately 6.75 volts (corresponding to a switch current of 67.5 amps), the PWM output goes low and does not reset until the beginning of the next pulse. Thus if the scaled load current drops below 6.75 volts, the PWM chip will be enabled at the beginning of the next pulse. This technique allows for some current to be delivered to the load, but still protects the IGBT from exceeding its rated values. Figure (5-13) shows the pulse-by-pulse feature as the scaled input load current is simulated to rise above the threshold value of 6.75 volts.

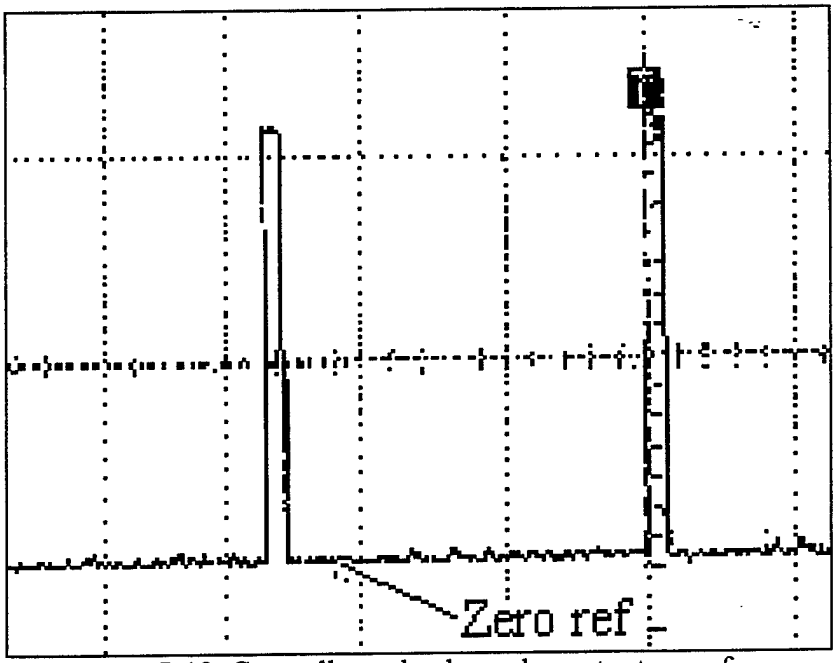


Figure 5-13, Controller pulse-by-pulse output waveform
20 μsec/div. CH1 input to driver signal 5V/div

3. Time Out Over-Current Protection

The second form of circuit protection is the over-current time out protection. This protects the circuit from thermal damage when the buck chopper is exposed to higher than rated currents for a specified period of time. This feature is invoked when the chopper exceeds 100% rated power and will follow a nonlinear time-out curve based on the extremity of the condition (See Figure 3-9). To simulate a time-out condition, a scaled voltage of 4.5 V was inserted into the $i_o/10$ buffer stage of the controller. This corresponds to an output current of 45 amps. This causes comparator U7 to send a positive voltage to $U5_2$ (See Figure (5-6)), causing its output to go high. When this occurs, the output of $U5_4$ will go to its high state and $U5_4$ sends a positive signal to comparator U8. When comparator U8 is sent the signal, its output goes high and sends a shutdown signal to pin 14 of the PWM chip. This signal disables the PWM until a reset momentary switch is pressed to clear the condition.

E. SINGLE BUCK CHOPPER OPERATION WITH FEEDBACK

With the protective circuitry and the proper PWM waveform verified, the jumper was removed and the buck chopper was placed in the control loop for testing. The criteria for testing the performance of the buck chopper are:

- Startup transient
- Load step change
- Input voltage perturbation

The tests are conducted with various resistive loads. Dynamic load testing attempts to imitate abrupt changes in load and facilitates the comparisons between laboratory results and simulation results.

1. Buck Chopper Startup and Ripple Rejection

Startup and ripple rejection laboratory results were obtained when the buck chopper was started with a 50Ω load (20% of rated power) attached. The buck chopper output voltage, AC (channel 1) and DC (channel 2), and the switch input voltage (AC coupled) were recorded for comparison to the simulated results. In order to minimize the noise introduced by a measurement device into the analog controller, the duty cycle output was not measured. Instead, the performance of the buck chopper may be evaluated by observing the output voltage. Figure (5-14) channel 3, clearly shows the buck chopper output voltage climbing and slowly approaches its steady-state value after 3 seconds. This is a result of the ramping of the duty cycle caused by the linear ramping up of the reference voltage. The switch input voltage, channel 2, drops as a result of the buck chopper load transient, but shows little ripple after the initial startup transient. The presence of less than 10 millivolts of AC coupled voltage on the output voltage (channel 1) after the transient shows that there is little communication of the rectification bank ripple voltage to the output voltage. This tends to show that the assumption and modeling of the prefilter was correct in that little low-frequency ripple reaches the load.

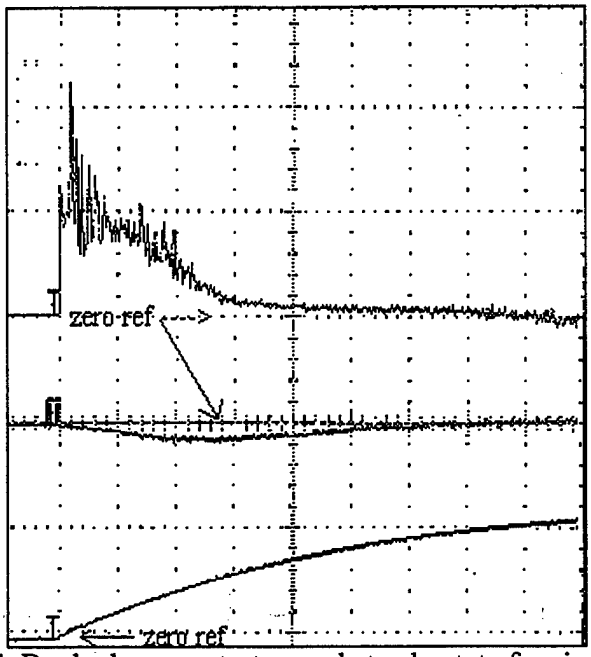


Figure 5-14, Buck chopper startup and steady state for ripple rejection 500ms/div UPPER (Vout) 100 mv/div. MIDDLE (Vin) 100mv/div LOWER (Vout (DC)) 300v/div

2. Source Voltage Droop

The consequence of adding a large load to the laboratory power distribution system was that the source voltage droops as a function of load. By repeating the startup transient, a correlation between load and voltage droop may be easily determined. It should be noted that the droop is not constant, but depends on overall load conditions at the time of the experiment. The experiment was performed at approximately 1300 on a workday afternoon and thus it is assumed to represent the typical droop characteristics for a work day. Figure (5-15) shows channel 1 (AC coupled output voltage), channel 2 (DC coupled switch input voltage) and channel 3 (DC coupled load current). By comparing the changes in switch input voltage to load current, the droop characteristic can be

obtained. The source voltage sags from 425 V to a terminal value of 405 volts, while the load current rises from zero to 6 amps, the resultant slope depicted on channel 2 is linear and is determined to be 3 volts per amp of load current.

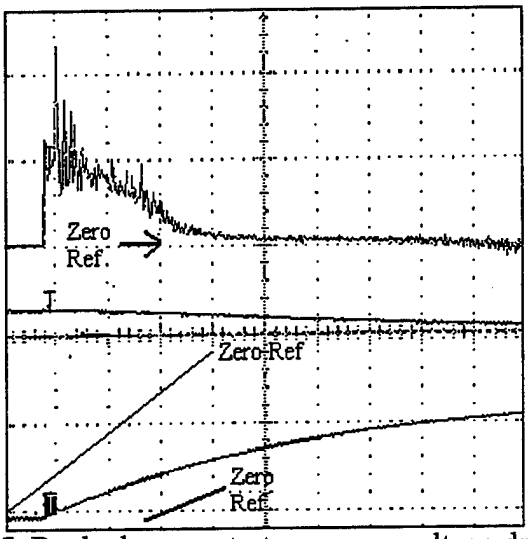


Figure 5-15, Buck chopper startup source voltage droop
500ms/div UPPER (Vout) 1 v/div. MIDDLE (Vin) 100v/div LOWER (Iout (DC)) 5a/div

3. Load Regulation

The final closed-loop circuit test performed was the load step changes. Prior to conducting these tests, the controller gains were reevaluated. Although the values incorporated in the initial design had provided excellent response characteristics, it was found that excessive voltage gain in the control feedback resulted in a large amount of output voltage noise. To provide excellent response characteristics without excessive voltage feedback, the gain values of Equation (4-33) were modified on the controller to:

$$h_i = 0.045 \qquad (5\text{-}7)$$

$$h_v = 0.01$$

$$h_n = .404$$

After these modifications were implemented on the control board, evaluation resumed. To test the buck choppers in a dynamic load environment, load banks were arranged such that one set would run continuously at 50% of the rated power while a second load bank was intermittently placed on and off line by means of pulsed inverter bank. This configuration was able to mimic a cyclic variation from 50% to 100%. Figure (5-16) shows the independent transient response of the paralleled buck choppers for the cycled step changes in load. The left panel illustrates the response of the master buck chopper, so named because its controller sets the switching frequency for both. The right panel represents the slave buck chopper. On either buck chopper, there is no current overshoot (lower figure) and the settling time is identical for both buck choppers for both the higher and lower-resistance steps. Once again, the feedback loop was able to eliminate the undesired overshoot. Although the simulations were computed with different gains, the results were similar.

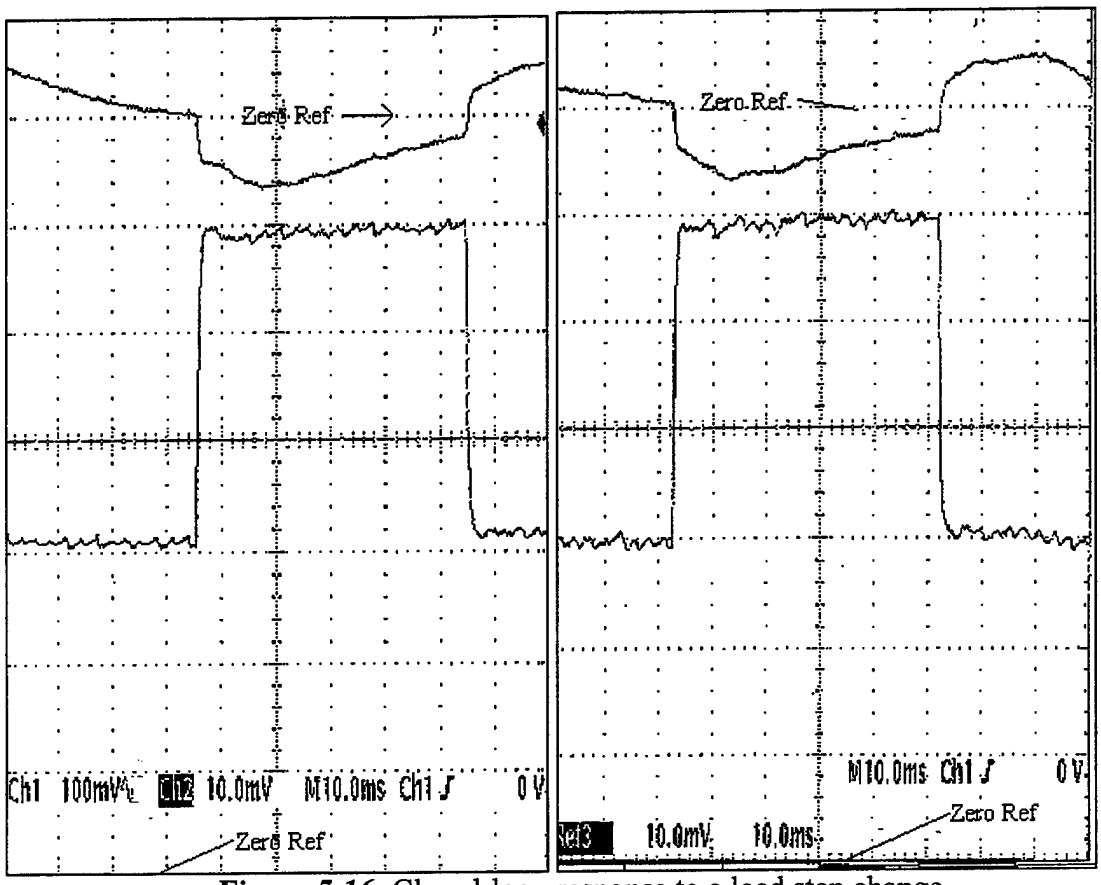


Figure 5-16, Closed-loop response to a load step change 10ms/div(Both Panels) UPPER (Vout(AC coupled)) 5 v/div. LOWER (Iout (DC)) 5a/div(Both Panels)

With both buck choppers responding to a load change in a virtually identical manner, the buck choppers were readied for parallel operation.

F. PARALLEL OPERATIONS

The buck choppers will first be tested in parallel ensuring the startup circuitry provides a smooth transition between single chopper operation and parallel operation. To do this the buck chopper startup circuitry will be tested by placing a buck chopper on-line

and starting the second buck chopper to validate the startup sequence. The last phase of testing will investigate the sharing of a dynamic load.

1. Buck Chopper Startup

In order to demonstrate a startup, the load current produced by each buck chopper is monitored. To see how well load is shared, load current of each are directly compared. In addition to load sharing, the output voltage should not undergo any rapid perturbations. Figure (5-17) shows the startup results with the lower curve representing the current output of the on-coming buck chopper and the middle curve representing the current output of the on-line machine. The response was compressed in order to provide the detail necessary to show the transient effects of starting a second buck chopper. As was shown in the model, the oncoming machine's output is delayed by approximately 3.5 seconds as the value of the negative small-signal portions of the control equation (3-37) decay away. After approximately 3 seconds, the startup circuit works with the controller to produce a positive duty cycle for the oncoming machine. The resultant trace shows that the oncoming buck chopper rapidly assumes load, while the on-line buck chopper rapidly sheds load . following this initial delay in the second machine assuming load, an additional 70 milliseconds is required before the two machines share load evenly. Figure (5-18) shows the slight amount of circulating current between the two capacitors. This circulating current is caused by a slight voltage differential between the output filters of the respective buck choppers. This effect is further amplified by compressing the time

scale. The time scale is compressed in order to fit as much of the startup sequence on the figure as possible without losing the key details of the transient.

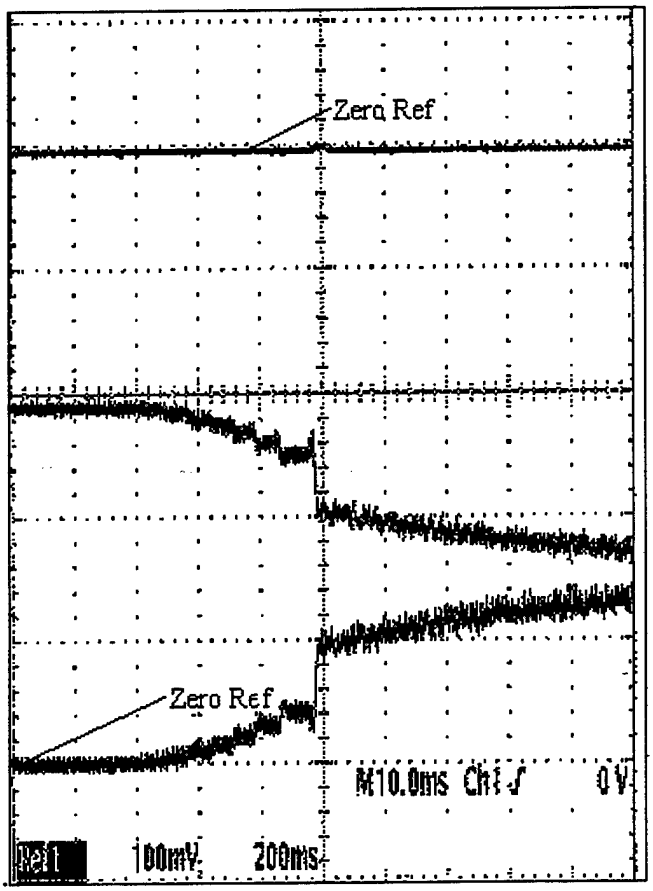


Figure 5-17, Paralleling a set of buck choppers UPPER (Vout(AC coupled)) 1 v/div.
MIDDLE- ONLINE BUCK(Iout (DC)) 5a/div
LOWER ONCOMING BUCK (Iout (DC)) 5a/div

The output voltage was AC coupled to show that the rapid assumption and shedding of load by the two choppers has no effect on the AC component of the output voltage. The output voltage (DC coupled) was shown to rise when lowering the load. This follows the prediction of the model and validates the utilization of the house curve. Finally, the two choppers are shown sharing the load.

2. Load Regulation

The final test run of the parallel combination of buck choppers was the dynamic load test. The test set-up was the same as that outlined in the single buck chopper section where the load was cycled between 50% and 100% of full power. The lower value was selected to ensure sufficient load was on each machine to avoid discontinuous operation during the lower load period. The upper limit was selected to ensure that the laboratory power distribution system was able to deliver the load without forcing either buck chopper to operate at 100% duty cycle. Figure (5-19) shows the combined response to the outlined load change. The upper curve shows the output voltage AC coupled for transient analysis. Due to the house curve effect, it is expected that the output voltage would lower as additional load is added and would rise as that load was taken off. Thus the voltage waveform for the analysis is similar despite different gain values between the two comparisons. This is because the house curve portion of the model is very close to the existing house curve incorporated in the controller. The middle curve represents the load current produced by the master buck chopper. It is offset by approximately 10 amps from the waveform produced by the slave buck chopper in order to clarify the picture and provide better resolution to the reader. Both load currents are seen to be approximately 7.5 amps prior to the addition of load and then 15 amps after the load. Transition from the low-load to high-load state is made within the model criteria of 15-20 milliseconds. Likewise the transition back to a low-load state shows that each chopper is capable of reaching the steady-state value within 15-20 milliseconds. Each of the two current waveforms show the effects of the circulating current that was previously discussed, but

in Figure (5-18) these effects are much more apparent. The current circulating between the two capacitors appears as a rise on one curve and an inverted depression on the other curve.

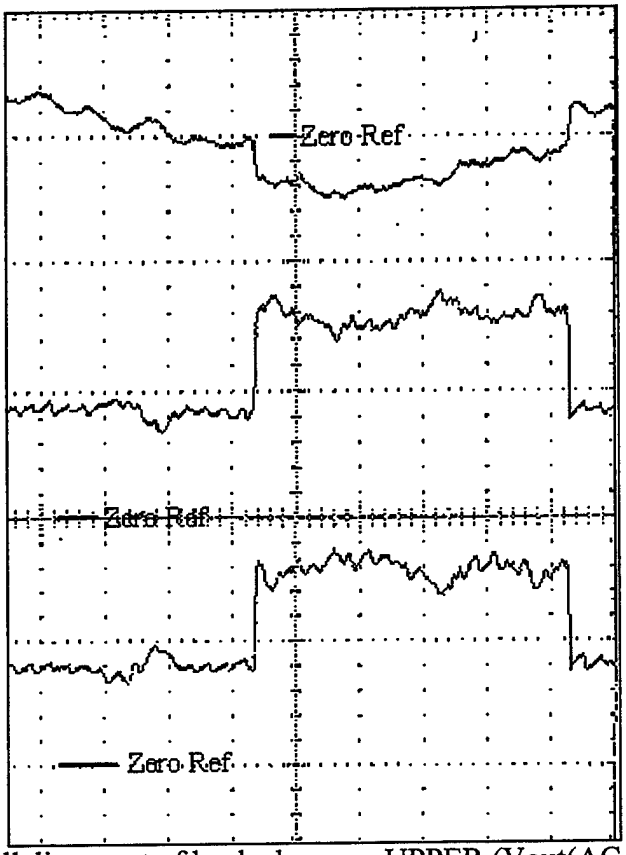


Figure 5-18, Paralleling a set of buck choppers UPPER (Vout(AC coupled)) 1 v/div. MIDDLE- ONLINE BUCK(Iout (DC)) 5a/div LOWER ONCOMING BUCK (Iout (DC)) 5a/div

With testing completed and summarized Chapter VI outlines the principle conclusions derived from this work and sets forth recommendations for further areas of investigation.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY OF RESULTS

The ability of the state-difference feedback with feed-forward to properly control the buck chopper has been established, but how does the controller measure up to the criteria for the research listed in the introduction? The first requirement was to show that the buck chopper could be started with a load between 10%-100% without initiating any protective features or any additional operating restrictions. The model and prototype both showed that this could be achieved without any special operating instructions. The startup procedure simply consists of connecting a suitable load to the output of the chopper, providing a 400 VDC supply voltage, energizing the controller and pressing the start button.

The second requirement was that the technique would allow quick response to transient load changes. In regards to fast dynamic response to changes in the control signal, the controller was able to respond to the change within 1 millisecond. The controller with power section achieved the steady-state operation within 20 ms of the imposition of the transient. The limiting element in dynamic response does not lie within the controller, but rather the power circuit being controlled due to the filter response. To achieve the high response speeds of the power section, the output filter of the buck chopper must be redesigned to allow for quicker response. The rather large size of the output filter capacitor hindered the response of the power section to rapid load changes. To enhance controller response, the 2000 μF output capacitor was replaced with a 230 μF

capacitor. The gain values were then reevaluated with the new component values. The resulting gains are:

$$h_i = 0.1 \qquad (6\text{-}1)$$

$$h_v = 0.05$$

$$h_n = 10$$

and produce the dominant control pole at 750 Hz. The dynamic response to a load change now occurs in less than 1 millisecond. This is a vast improvement over the previous selection of gain values. With the dominant control pole at 750 Hz and the prefilter pole at 172 Hz, there is a small possibility of interaction between the two. The replacement of the 2000μF capacitor of the prefilter with a 7700μF capacitor, moves the filter pole to 82 Hz. This is close enough to a decade away from the control pole to ensure that there will be no interaction between the two. Furthermore, the prefilter gain at 360 Hz is -24 dB. This is a marked improvement over the -10 dB of the original configuration and will virtually eliminate all of 360 Hz ripple to the input of the switch.

The control pole location of 750 Hz has an additional benefit. During laboratory testing a 60 Hz subharmonic was found on the 3-phase rectified laboratory supply power. This is due to the buildings electrical distribution system phase loading mismatch. With this exceptionally unbalanced configuration, a subharmonic voltage fluctuation is introduced between the two operating phases and is manifested in 60 Hz ripple on the rectified laboratory supply voltage. Since the dominant control pole is greater than a

decade above the 60 Hz ripple, we did not expect any interaction between the two and final bench testing proved this assumption to be correct.

The next requirement was to demonstrate the ability of the control routine to allow the buck choppers to share load when in parallel. Recall that during the startup portion of the parallel operation testing, a circulating current was detected between the two capacitors. This action results from the use of two different inductance values on the post filter of the buck chopper. During the switch 'on' time, the buck chopper with the higher inductance builds up capacitor voltage at a slower rate than the other buck chopper. Thus, with a voltage differential between the two capacitors, current flows from the buck chopper that has the higher voltage to the one that has the higher inductance value. During the switch 'off' period, the buck chopper with the higher inductance will lose its output voltage at a slower rate than the other buck chopper, thus current will flow from the capacitor of the buck chopper with the higher inductance to the other buck chopper and complete the cycle of the circulating current. An easy solution to this phenomena may be realized by reducing the lead length between the outputs of the two converters. This will minimize the stray inductance and help reduce the circulating current. In so doing, the perturbations induced in the control cycle by the circulating current will also be reduced to a negligible amount.

Finally, the last requirement was to demonstrate rapid response and effective control for parallel buck choppers operating in a dynamic load environment. The buck choppers operating with the original gain values and original power sections were able to

achieve steady-state output voltage within 15 milliseconds when 50% additional load was added and removed cyclically.

B. FUTURE RESEARCH AREAS

With the rapid sampling and quick processing times, implementation of the algorithm on DSP boards available in the lab would make the controller more flexible. The algorithm or just the gains would be software changeable.

1. Digital Signal Processing Application

The processing power of modern DSP chips makes the implementation of more complex control algorithms possible. The speed at which the DSP controller can switch a power converter is also increasing. The advantages of implementing the control on a DSP board are flexibility, simplicity, and reproducibility. The control technique in this thesis would require only simple arithmetic computations in software. The benefit (of DSP control implementation) is the possibility of a rapid and accurate reproducibility, which would be quite difficult to implement in the current prototype controller. This would ensure that each buck chopper had the exact same gain values, behaved throughout its life in the same manner and was insensitive to minor variations in temperature. With rapid processing speeds, it becomes possible to reevaluate the computed duty cycle at a rate in excess of the switching frequency. This would allow for exceptionally fast control with the current limitations of the buck chopper only being the 'headroom' of the steady-state duty cycle and 'softness' of the supply power.

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APPENDIX A. IGBT DATA SHEETS

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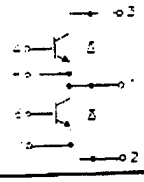
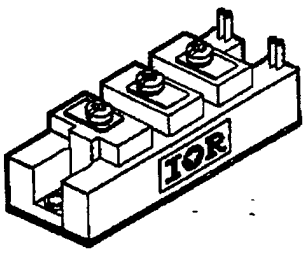


V_{CE} = 600V

I_C = 90A

V_{CE}(ON) < 3.0V

- Rugged Design
- Simple gate-drive
- Ultra-fast operation up to 25KHz hard switching, or 100KHz resonant
- Switching-Loss Rating includes all "tail" losses



INT-A-PAK case

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Absolute Maximum Ratings

Parameter	Description	Value	Units
V_{CES}	Continuous collector to emitter voltage	600	V
I_C @ T_C = 25°C	Continuous collector current	90	A
I_C @ T_C = 85°C	Continuous collector current	60	
I_C @ T_C = 100°C	Continuous collector current	50	
I_{LM}	Peak switching current	180	
I_{FM}	Peak diode forward current (1) 225		
V_{GE}	Gate to emitter voltage	± 20	V
V_{ISOL}	RMS isolation voltage, any terminal to case, t= 1 min	2500	
P_D @ T_C = 25°C	Power dissipation	298	W
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-40 to 125	

(1) Duration limited by max junction temperature.

Electrical Characteristics - T_J = 25°C, unless otherwise stated

Parameter	Description	Min	Typ	Max	Units	Test Conditions
BV_{CES}	Collector-to-emitter breakdown voltage	600	—	—	V	V_{GE} = 0V, I_C = 1mA
V_{CE}(ON)	Collector-to-emitter voltage	—	—	3.0		V_{GE} = 15V, I_C = 90A
		—	3.1	—		V_{GE} = 15V, I_C = 90A, T_J = 150°C
V_{FM}	Diode forward voltage - maximum	—	—	2.8		I_F = 90A, V_{GE} = 0V
		—	2.6	—		I_F = 90A, V_{GE} = 0V, T_J = 150°C
V_{GEth}	Gate threshold voltage	3.0	—	5.5		I_C = 500µA
ΔV_{GEth}	Threshold voltage temperature coeff.	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 500µA
g_{fe}	Forward transconductance	34	—	58	S(℧)	V_{CE} = 25V, I_C = 90A
I_{CES}	Collector-to-emitter leakage current	—	—	1	mA	V_{GE} = 0V, V_{CE} = 600V
		—	—	10		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-emitter leakage current	—	—	±1	µA	V_{GE} = ±20V

Dynamic Characteristics - T_J = 150°C

Parameter	Description	Min	Typ	Max	Units	Test Conditions
E_{on}	Turn-on switching energy	—	0.05	—	mJ/A	R_{G1} = 47Ω, R_{G2} = 0Ω
E_{off} (1)	Turn-off switching energy	—	0.05	—		I_C = 90A, L_S = 100nH
E_{ts} (1)	Total switching energy	—	—	0.12		V_{CC} = 360V, V_{GE} = ± 15V
$t_{d(on)}$	Turn-on delay time	—	70	—	ns	R_{G1} = 47Ω, R_{G2} = 0Ω
t_r	Rise time	—	90	—		I_C = 90A
$t_{d(off)}$	Turn-off delay time	—	180	—		V_{CC} = 360V, V_{GE} = ± 15V
t_f	Fall time	—	250	—		L_S = 100nH
I_{rr}	Diode peak recovery current	—	52	—	A	R_{G1} = 47Ω, R_{G2} = 0Ω
t_{rr}	Diode recovery time	—	110	—	ns	I_C = 90A
Q_{rr}	Diode recovery charge	—	3.0	—	µC	V_{CC} = 360V, V_{GE} = ± 15V
Q_{ge}	Gate-to-emitter charge (turn-on)	150	—	280	nC	V_{CC} = 360V
Q_{gc}	Gate-to-collector charge (turn-on)	70	—	140		I_C = 90A
Q_g	Total gate charge (turn-on)	26	—	42		V_{GE} = 15V
C_{ies}	Input capacitance	—	5800	—	pF	V_{GE} = 0V
C_{oes}	Output capacitance	—	660	—		V_{CC} = 30V
C_{res}	Reverse transfer capacitance	—	80	—		f = 1MHz

(1) Includes tail losses

Thermal and Mechanical Characteristics

Parameter	Description	Typ	Max	Units
R_{thJC} (IGBT)	Thermal resistance, junction to case, each IGBT	—	0.42	°C/W
R_{thJC} (Diode)	Thermal resistance, junction to case, each diode	—	0.7	
R_{thCS} (Module)	Thermal resistance, case to sink	0.1	—	
Wt	Weight of module	140	—	g

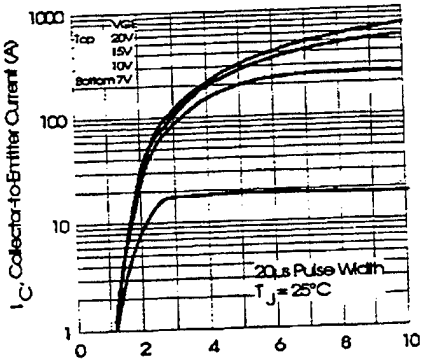

Fig. 1 - Typical Output Characteristics, T_J = 25°C

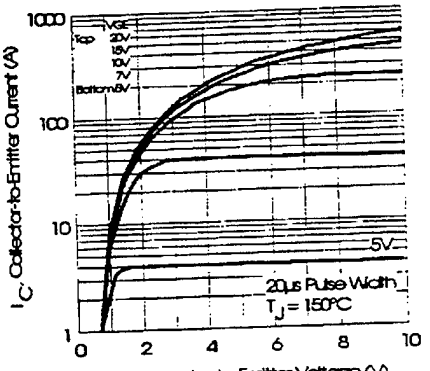

Fig. 2 - Typical Output Characteristics, T_J = 150°C

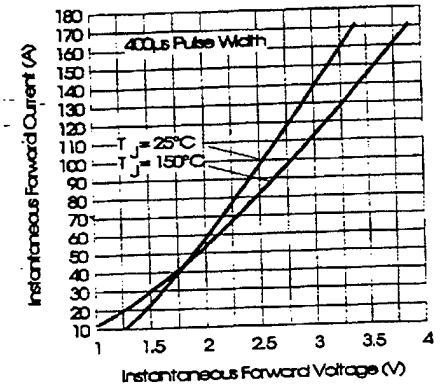

Fig. 3 - Typical Output Characteristics

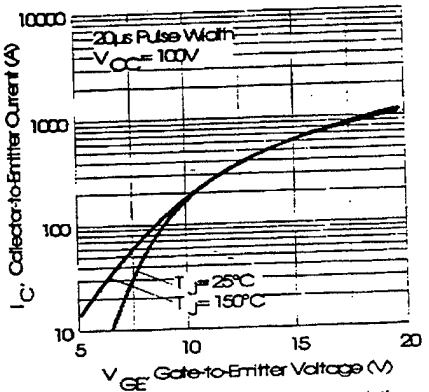

Fig. 4 - Typical Transfer Characteristics

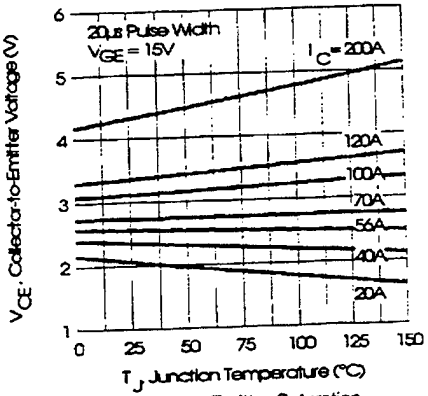

Fig. 5 - Collector-to-Emitter Saturation Typical Voltage vs. Junction Temperature

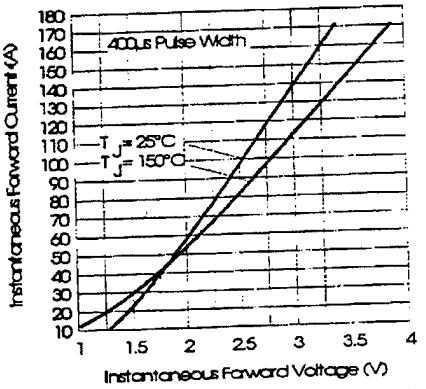

Fig. 6 - Forward Voltage Drop Characteristics

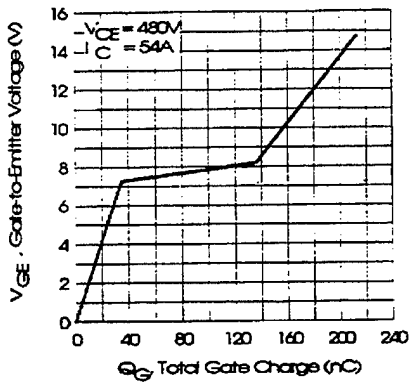

Fig. 7 - Typical Gate Charge vs. Gate-to-Emitter Voltage

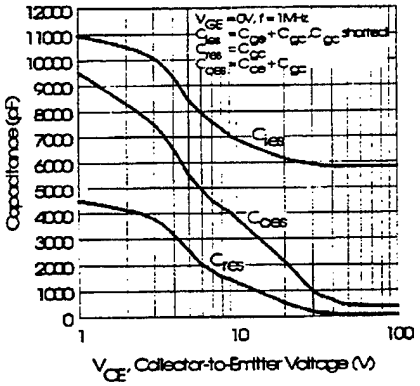

Fig. 8 - Typical Capacitance vs. Collector-to-Emitter Voltage

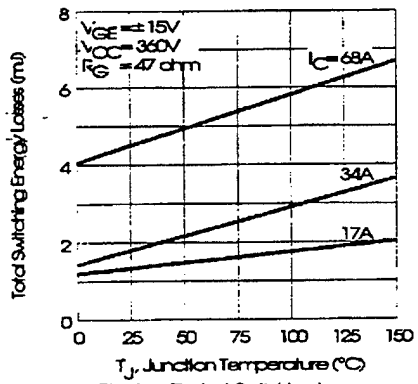

Fig. 9 - Typical Switching Losses vs. Junction Temperature

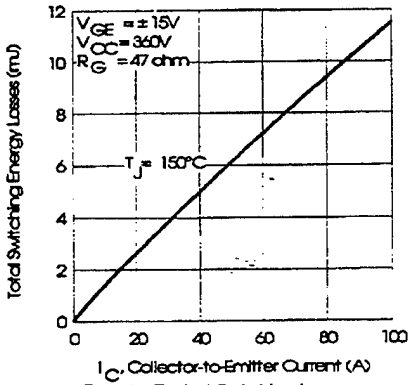

Fig. 10 - Typical Switching Losses vs. Collector-to-Emitter Current

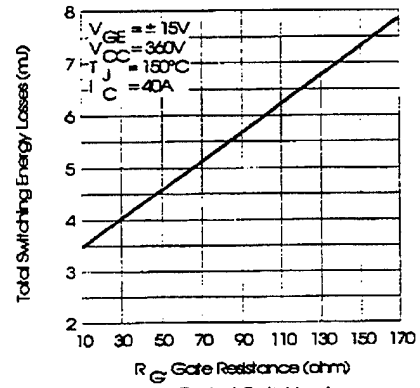

Fig. 11 - Typical Switching Losses vs. Gate Resistance

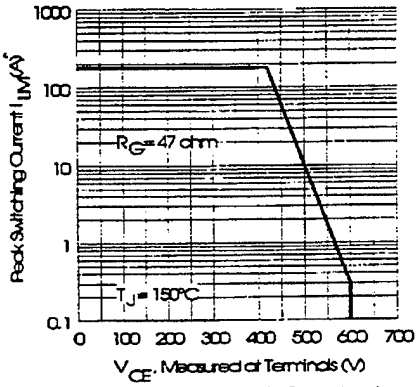

Fig. 12 - Reverse Bias Safe Operating Area

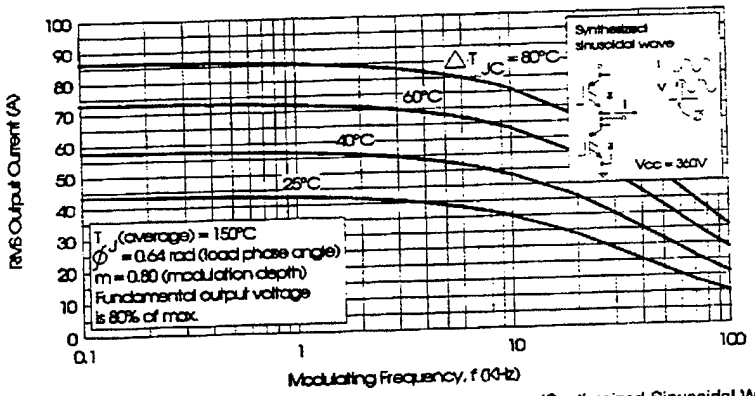

Fig. 13 - Typical RMS Output Current per phase vs. Frequency (Synthesized Sinusoidal Wave)

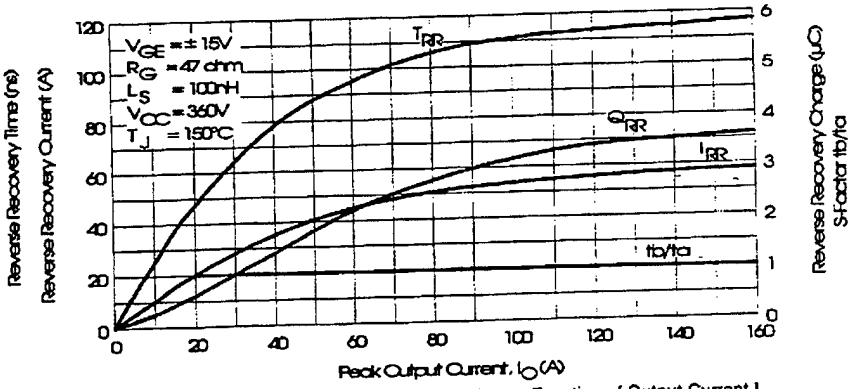

Fig. 14 - Typical Diode Recovery Characteristics as Function of Output Current I_O

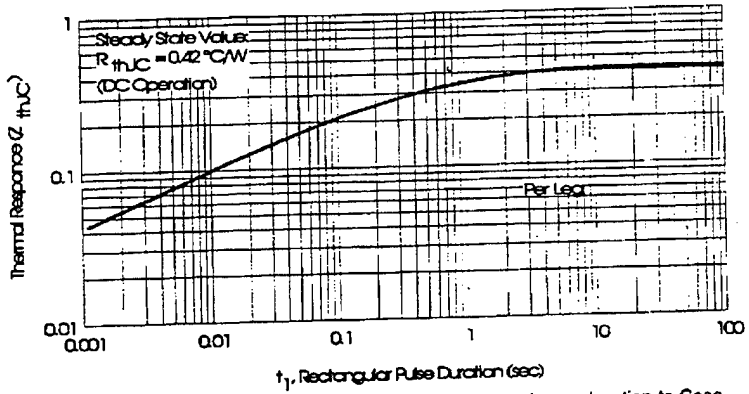

Fig. 15 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

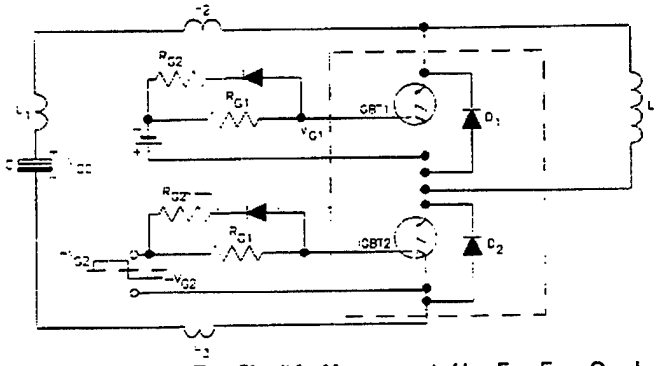

Fig. 16 - Test Circuit for Measurement of I_{LM}, E_{ON}, E_{OFF}, Q_{RR}, I_{RR}, $t_{D(ON)}$, t_r, $t_{D(OFF)}$, t_f

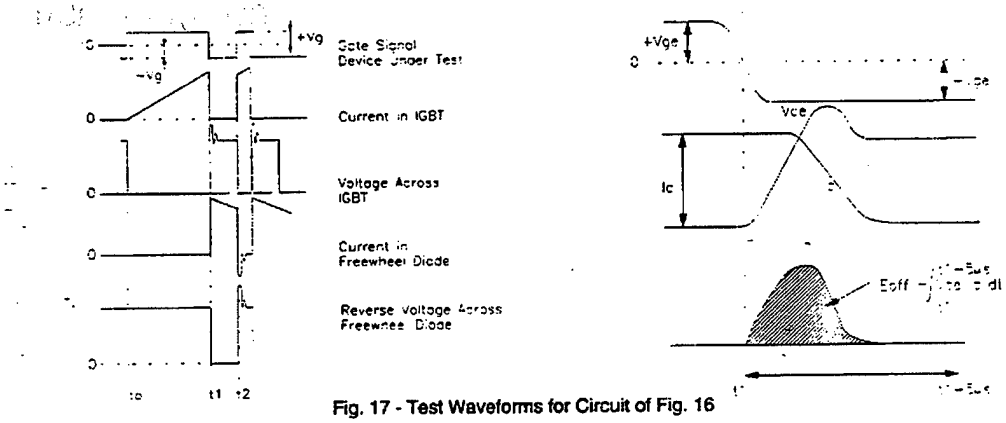

Fig. 17 - Test Waveforms for Circuit of Fig. 16

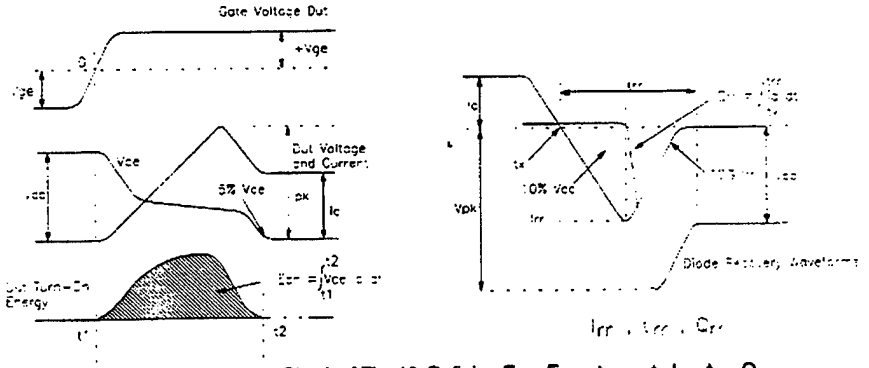

Fig. 18 - Test Waveforms for Circuit of Fig. 16, Defining E_{ON}, E_{REC}, $t_{D(ON)}$, t_r, I_{RR}, t_{RR}, Q_{RR}

APPENDIX B. MATLAB SIMULATION CODE

The process of simulating the model using the following m-files is illustrated in Figure (B-1).

```
%************************************************ buckcons.m
% Determining Buck Circuit Parameters
% Specifications: 90 A IGBT's
% Analog controller patterned after SSCM.
% Want fres << fline = 360 Hz.
% Want continuous operations between 10% and 100% loading.
% Simulation sequence cycles through startup -> 10% loading -> full loading.
% Last mod:  15 Feb 97
%************************************************
% Constant Definitions
E     = 400.0;          % input voltage of buck
Vcd   = 305.0;          % desired output voltage of buck: 10%
Pout  = 9e3;            % output power
Cf    = 2000e-6;        % chosen based on fres << fline & parts
Lfilt = 0.425e-3;       % actual filter inductance value
Cfilt = 2000e-6;        % actual filter capacitance value
rx_full = (Vcd^2)/Pout;     % low R value  - full load current
rx_ten  = (Vcd^2)/(0.1*Pout); % high R value - 10% load current
rxstart = rx_ten;       % starting resistance
d     = Vcd/E;          % duty cycle
fline = 360.0;          % 360 Hz ripple from 6 pulse rectifier
f     = 18e3;           % switching frequency
T     = 1/f;            % switching period
pw    = d*T;            % pulse width for switching noise SS model
%************************************************
% Menu bar choices to allow open loop and                *
% closed loop testing of buck chopper #1 and #2.         *
% Two choices for buck choppers since each has           *
% different main inductor value.                         *
%************************************************
k = menu('Choose Simulation','760 uH Buck: Open Loop','875 uH Buck: Open
Loop','760 uH Buck: Closed Loop','875 uH Buck: Closed Loop');
if (k == 1)
  flag = 0;             % flag = 0 --> open loop simulation
  L = 0.760e-3;         % actual inductance value for buck 1 (3 stack)
  elseif (k == 2)
  flag = 0;         % flag = 0 --> open loop simulation
  L = 0.875e-3;     % actual inductance value for buck 2 (2 stack)
elseif (k == 3)
  flag = 1;         % flag = 1 --> closed loop simulation
```

```
  L = 0.760e-3;       % actual inductance value for buck 1 (3 stack)
elseif (k == 4)
  flag = 1;           % flag = 1 --> closed loop simulation
  L = 0.875e-3;       % actual inductance value for buck 2 (2 stack)
end
% end if
%************************************************
% Determination of Lcrit: low load R determines                *
R    = rx_ten;                    %                              *
Lcrit = (T*R/2)*(1-d);   % critical inductance                  *
% Determination of delta_I, Imax, Imin, ILavg                  *
% and I_load at 10% load (ll).                                 *
%************************************************
delta_I  = ((E - Vcd)/L)*d*T;
Imax_ll  = d*E*(1/R + (1-d)*T/(2*L));    % ll max L current
Imin_ll  = d*E*(1/R - (1-d)*T/(2*L));    % ll min L current
ILavg_ll  = (Imax_ll+Imin_ll)/2;         % ll avg L current
I_load_ll = Vcd/R;                       % ll current
%************************************************
% Determination of Imax, Imin, ILavg                           *
% and I_load at full load (fl).                                *
%************************************************
R     = rx_full;
Imax   = d*E*(1/R + (1-d)*T/(2*L));    % fl max L current
Imin   = d*E*(1/R - (1-d)*T/(2*L));    % fl min L current
ILavg  = (Imax+Imin)/2;llll=475e-6;    % fl avg L current
I_load  = Vcd/R;                       % fl current
%************************************************
% Determination of resonant peak for L / Cf LPF.               *
%************************************************
fres =1/(2*pi*sqrt(L*Cf));
%************************************************
% Determination of resonant peak for                           *
% input Lfilt / Cfilt LPF.                                     *
%************************************************
fres_filt = 1/(2*pi*sqrt(Lfilt*Cfilt));
```

```
%************************************************
%buckstrt.m
% Provides startup parameters for 9 kW, 18 kHz
% buck chopper. Calls buckcons.m, a constant
% file developed for above buck chopper.
% Last mod:  18 Feb96
%************************************************
clear   % clear MATLAB memory
buckcons
% establish buck constants
%************************************************
% Pole specifications
%************************************************
%poles=[-10681.4+0.0*i,-925.0+534.1*i,-925.0-534.1*i];
poles = [-15000,-1500,-1500];
% desired characteristic polynomial;
S=poly(poles);
%************************************************
% Gain calculations:  Calculated using low starting
% resistance.  Gains are utilized as
% first run starting point.  Entry of manual
% gains can follow to give best overall
% response over all operating conditions.  Use
% board resistors in practice to set gains.
%************************************************
R = rxstart;hi = ((L*R*Cf*S(2))-L)/(E*R*Cf);
hn = (L*Cf*S(4))/E + hi*L/2;
hv = ((L*R*Cf*S(3))-(E*hi)-R)/(E*R);
%hi=0.05;
% manual gain entry;
hi = 0.05;hn = 1;hv =0.2;
%************************************************
% Function to verify poles obtained with gains
% match desired poles.
%************************************************
Am = [ 0        -1/L                  E/L;
    1/Cf      -1/(R*Cf)             0;
   -hv/Cf     (hi/L)+(hv/(R*Cf))-hn    -hi*E/L ];
syspole = eig(Am);    % check for correct poles
%************************************************
% SIMULINK no load parameters (are in addition
% to constants determined in buckcons.m)
%************************************************
```

```
% ABCD state space parameters
A = [ -1/(R*Cf)  1/Cf ;     -1/L      0    ];
B = [ 0;     E/L ];C = [ 1 0;     0 1 ];
D = [ 0;    0];
%************************************************
% Update initial conditions for integrators
%************************************************
Vciv    = 0;       % initial Vc integrator value
iLiv    = 0.0;      % initial hn integrator value
hnintiv  = 0.0;      % initial hn integrator value
tstart   = 0.0;      % simulation start time
tstop    = 1.25;     % simulation stop time
% ABCD state space parameters
```

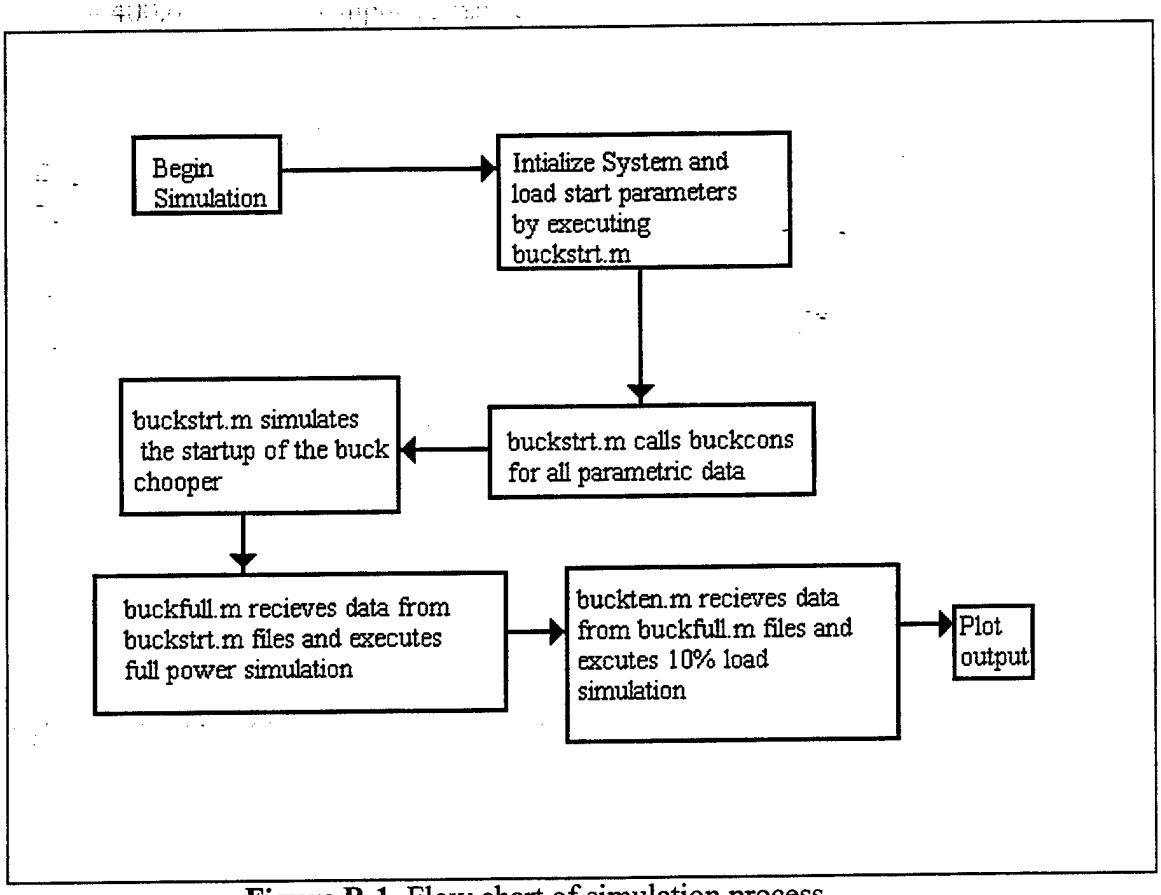

Figure B-1, Flow chart of simulation process

```
%buckfull.m                                          *
%                                                    *
% Provides full load parameters for 9 kW,            *
% 18 kHz buck chopper.                               *
%                                                    *
% Last mod:  15 Feb97                                *
%****************************************************
R = rx_full;    % full load resistance value
%****************************************************
% Function to verify poles obtained with gains       *
% match desired poles.                               *
%****************************************************
Am = [ 0        -1/L                E/L
     1/Cf     -1/(R*Cf)              0
    -hv/Cf    (hi/L)+(hv/(R*Cf))-hn   -hi*E/L ];
syspole = eig(Am);    % check for correct poles
%****************************************************
% SIMULINK no load parameters (are in addition       *
% to constants determined in buckcons.m)             *
%****************************************************
% ABCD state space parameters
A = [ -1/(R*Cf)  1/Cf
    -1/L       0   ];
B = [ 0;     E/L ];C = [ 1 0;     0 1 ];D = [ 0;     0];
%****************************************************
% Data passdown before buckfull.m simulation         *
% begins.                                            *
%****************************************************
Vc_response = Vc;
iL_response = iL;
timer = time;
d_response=d;
vswitch_response=Vswitch;
%****************************************************
% Update initial conditions for integrators in       *
% buckfull.m simulation.                             *
%****************************************************
Vciv   = Vc(length(time));
% Vc initial value for buckfull.m
iLiv   = iL(length(time));
% iL initial value for buckfull.m
tstart  = tstop;
% sim. start time for buckfull.m
```

```
tstop    = tstop + .5;
% simulation stop time for buckfull.m

%*********************************************
% This block only executes when cloosed loop      *
% simulation selected. Flag value in buckcons.m.  *
% This block allows passdown and updating         *
% of values as done above for Vc and iL.          *
%*********************************************
if ((k == 3)|(k ==4))
  hnint_response = [ hnint_response; hnint];
  % hnintiv initial value for buckfull.m
  hnintiv = hnint(length(time));
end   % end if
```

```
%************************************************
% buckten.m                                      *
%                                                *
% Provides 10% load parameters for 9 kW, 18 kHz  *
% buck chopper.                                  *
%                                                *
%                                                *
% Last mod:  17FEB97                             *
%************************************************
R = rx_ten;
% 10% load resistance value
%************************************************
% Function to verify poles obtained with gains   *
% match desired poles.                           *
%************************************************
Am = [ 0        -1/L              E/L;
     1/Cf     -1/(R*Cf)            0;
    -hv/Cf    (hi/L)+(hv/(R*Cf))-hn   -hi*E/L ];

syspole = eig(Am);    % check for correct poles
%************************************************
% SIMULINK no load parameters (are in addition   *
% to constants determined in buckcons.m)         *
%************************************************
% ABCD state space parameters
A = [ -1/(R*Cf)  1/Cf ;     -1/L      0   ];
B =[ 0;    E/L ];
C = [ 1 0;     0 1 ];
D = [ 0;     0 ];
%************************************************
% Data passdown before buck_ten.m simulation     *
% begins.                                        *
%************************************************
Vc_response   = [ Vc_response; Vc];
iL_response   = [ iL_response; iL];
d_response    = [ d_response; d];
timer         = [ timer; time];
vswitch_response=[vswitch_response;Vswitch];
%************************************************
% Update initial conditions for integrators for  *
% buckten.m simulation                           *
%************************************************
Vciv   = Vc(length(time));       % Vc initial value for buckten.m
iLiv   = iL(length(time));       % iL initial value for buckten.m
tstart = tstop;                  % simulation start time for buckten.m
```

```
tstop   = tstop +.50;          % simulation stop time for buckten.m
%************************************************
% This block only executes when cloosed loop      *
% simulation selected. Set flag value in          *
% buckcons.m.  This block allows passdown and     *
% updating of values as done above for Vc / iL    *
%************************************************
if ((k == 3)|(k ==4))
hnint_response = hnint;
hnintiv = hnint(length(time));  % hnintiv initial value for buckten.m

end   % end if
```

```
%************************************************
%                                                *
%                                                *
% Plot startup, change to 10% loading, & change  *
% to full loading for 9 kW, 17 kHz buck          *
% chopper.                                       *
%                                                *
% Last mod:  15 FEB 97                           *
%************************************************
Vc_response   = [ Vc_response; Vc ];
iL_response   = [ iL_response; iL ];
timer         = [ timer; time ];
d_response    = [d_response; d];
vswitch_response=Vswitch;
datastep = 40:1:length(timer);
% Allows plotting fewer points
% than generated.
figure(1)
subplot(3,1,1), plot(timer(datastep),Vc_response(datastep),'b'),
 grid;
if ((k == 1) | (k == 3))
  title('Vc, Switch input voltage, Duty Cycle vs Time: 760 uH Buck')
else
  title('VciL, Switch input voltage, Duty Cycle  vs Time: 875 uH Buck')
end
% end if
xlabel('time  (seconds)');ylabel('Vc(volts)');
subplot(3,1,2),
plot((time),vswitch_response,'b')
, grid

xlabel('time  (seconds)');ylabel('Switch Input Voltage(volts)');
subplot(3,1,3),
plot(timer(datastep), d_response(datastep),'b'); grid

xlabel('time  (seconds)');ylabel('Duty Cycle');
%************************************************
% If block only executes when closed loop        *
% simulation occurring.  Flag value set in       *
% buckcons.m.  This block sets final             *
% hnint_response vector and allows expansion     *
% for plotting.                                  *
%************************************************
if ((k == 3)|(k == 4))
  hnint_response = [ hnint_response; hnint ];
```

```
end
% end if hi hv hn
```

APPENDIX C. NETLIST CONTROLLER, PLL AND IGBT DRIVER CIRCUITS

The following pages detail the component value and netlist for the controller, Phase lock loop and IGBT driver circuits. A netlist is generated by the Protel EASYTRAX™ software and summarizes the relative location of parts on a printed circuit board. The software is used to implement a computer aided physical layout of part location and allows the designer a double check to ensure that the proper connections are made prior to manufacturing a PCB. Upon final review by the designer, the software is capable of creating a Gerber file, which may be utilized by computer aided mil machines to produce the printed circuit board. The netlist is a listing of those components connected at a specific location. Thus a netlist can aid during the manual population of the printed circuit board by providing a ready reference for part location.

NPS Documentation for Interim Analog Buck Chopper Controller

Table of Integrated Circuits with Descriptions

Symbol	Component	Description	Function in Circuit
U1	LF347	Quad Op Amp	Performs the main control law.
U2	LM324	Quad Op Amp	Buffer the signals from the current and voltage sensor.
U3	UC3637	PWM Controller	Converts duty cycle to a PWM signal.
U4	AD534	Voltage Multiplier	Determines the steady state duty cycle by analog division of the input voltage and reference voltage. Feedforward loop.
U5	7432	Quad OR Gate	Latches the protection circuit trips for over-current time-out and low control voltage.
U6	1458	Dual 741 Op Amp	Establishes the reference voltage and start-up ramp.
U7	LM311	Comparator	Used in conjunction with the op amp in U3 as an over-current time-out circuit.
U8	LM311	Comparator	Interfaces TTL output trip circuit with U3-14 shutdown pin.
U9	TWR-5/1000-15/1000-D12	+/-15V @200mA and +5V @1A DC-to-DC Converter	Converter a triangle wave to a 20% duty cycle square wave for the PLL.

Resistor, Capacitor and Diode Labeling

For the purpose of more easily locating components and understanding their function in the circuit, in general the following format was chosen:

The first digit represents the type of component.

R- resistor
C- capacitor
D- diode

The second digit represents the IC that it is best associated with.

0- U10
1- U1
2- U2
etc.

The third and forth digits are use for IC pin location.

03- pin 3
18- pin 18
etc.

If a suffix is used then there are generally more than one of the same components connect to the same pin.

A, B, C- Indicated multiple component of the same type connected to the same pin.
G- Ground
H- Vcc, Vdd
L- Vss
Q- Transistor

Here are several examples:

D317- This is a diode connected to U3 pin 17.
R113C- This is a resistor connected to U1 pin 13 and there are at least two more resistors connected to that same node.
C006- This is a capacitor connect to U10 pin 6.
RJ4036Q- This is a resistor connected to J40 pin 36 and a transistor. This symbol is an exception to the rule.

Vias and layout of the control board:

The board was layed out in EASYTRAX software and milled such that there are no isolated ground sections. There are 25 vias on the analog control board. Their location are on the lines connected to the following pins:

Pin	#Vias
+15V	7
-15V	7
+5V	1
J25-14	2
J25-24	1
U2-7	1
U3-4	2
U3-14	1
U4-12	1
U6-7	1
U7-7	1
Total	25

Connector Information

J25 - 25 pin D-sub connector that interfaces the controller with the signals from the PPI power portion.

Component List for the SSCM Prototype Analog Control Board

R411G AXIAL0.4	R803 AXIAL0.4	R102C AXIAL0.4	C305 RAD0.2
C603 RAD0.2	R803G AXIAL0.4	R101 AXIAL0.4	C804 RAD0.2
R603 AXIAL0.4	C107 RAD0.2	R113B AXIAL0.4	C808 RAD0.2
R603H AXIAL0.4	D107 DIODE0.4	R110 AXIAL0.4	C514 RAD0.2
R411 AXIAL0.4	D106 DIODE0.4	R102A AXIAL0.4	C708 RAD0.2
R607 AXIAL0.4	R112G AXIAL0.4	C203 RAD0.2	C704 RAD0.2
C902 RAD0.2	R114 AXIAL0.4	C210 RAD0.2	C306 RAD0.2
C905 RB.3/.6	R108 AXIAL0.4	C212 RAD0.2	C111 RAD0.2
C904 RB.3/.6	R110G AXIAL0.4	C205 RAD0.2	C104 RAD0.2
C907 RB.2/.4	R109 AXIAL0.4	R024J AXIAL0.4	C211 RAD0.2
C901 RB.2/.4	R102B AXIAL0.4	R203 AXIAL0.4	C204 RAD0.2
R112 AXIAL0.4	R113A AXIAL0.4	R205 AXIAL0.4	C608 RAD0.2
R807Q AXIAL0.4	R113C AXIAL0.4	R210 AXIAL0.4	C414 RAD0.2
R807H AXIAL0.4	R106 AXIAL0.4	R212 AXIAL0.4	C408 RAD0.2
R606 AXIAL0.4	R313 AXIAL0.4	C904D RAD0.2	C604 RAD0.2

D901A
DIODE0.4

D902A
DIODE0.4

D901B
DIODE0.4

D902B
DIODE0.4

R902
AXIAL0.4

R907
AXIAL0.4

D907
RAD0.1

R313G
AXIAL0.4

R704
AXIAL0.4

R702
AXIAL0.4

R316B
AXIAL0.4

R316A
AXIAL0.4

R318
AXIAL0.4

R301
AXIAL0.4

R311
AXIAL0.4

C313
RAD0.2

C301
RAD0.2

C311
RAD0.2

C302
RAD0.2

C317
RAD0.2

C702
RAD0.2

D311
DIODE0.4

D301
DIODE0.4

D317
DIODE0.4

R501
AXIAL0.4

R509
AXIAL0.4

R504
AXIAL0.4

R807
AXIAL0.4

R505
AXIAL0.4

R502
AXIAL0.4

C807
RAD0.2

C501
RAD0.2

C803
RAD0.2

C316
RAD0.2

R603V
VR1

C907G
RAD0.2

U1
DIP14
LF347

U2
DIP14
LM324

U3
DIP18
UC3637

U4
DIP14
AD534

U5
DIP14
7432

U6
DIP8
1458

U7
DIP8
LM311

U8
DIP8
LM311

U9
DATEL
TWR-5/1000-
15/200-D12

Q1
TO-92A
2N2222

J25
DB25RA/F

Net List for the PEBB Buck Prototype Analog Control Board

NET1
R411G-2
R411-1
U4-11
)
(
NET2
C603-2
U6-3
R603-2
Q1-3
)
(
NET3
U6-1
U6-2
R606-2
)
(
NET4 (-15V)
U6-4
C905-2
C904D-1
C305-2
C804-2
C704-2
C111-2
C211-2
C408-1
C604-2
U3-5
U7-4
U8-4
U2-11
U4-8
U9-5
U1-11
R704-1
R316A-2
R318-2
C316-2
)
(
NET5
U6-6
R607-2
R606-1
)
(
NET6 (Vref)
U6-7
R607-1
R102B-1
U4-10
)
(
NET7 (+15V)
U6-8
R603H-1
C904-1
R807H-2
R803-1
R313-1
C904D-2
C808-1
C708-2
C306-2
C104-1
C204-1
C608-1
C414-1
U3-6
U7-8
U8-8
U2-4
U4-14
U9-4
U1-4
R301-1
C807-1
)
(
NET8
R603-1
R603V-2
)
(
NET9
R603H-2
R603V-1
)
(
NET10 (io/10)
R411-2
R109-1
R102A-1
U2-13
U2-14
R316B-2
)
(
NET11
C902-2
C901-2
U9-2
D902A-A
D902B-A
R902-1
)
(
NET12
C902-1
C901-1
U9-1
D901A-K
D901B-K
)
(
NET13 (+5V)
C907-1
C514-1
U5-14
U9-7
J25-4
R907-2
R504-2
C501-2
C907G-1
)
(
NET14
R112-1
R106-2
R101-2
U1-1
)
(
NET15
R112-2
R112G-1
U1-12
)
(
NET16
R807Q-1
U8-7
R807-2
)
(
NET17
R807Q-2
Q1-2
)
(
NET18
R807H-1
U3-14
R807-1
C807-2
)
(
NET19
R803-2
R803G-2
U8-3
C803-2
)
(
NET20
C107-2
D107-A
R113C-2
U1-7
)
(
NET21

C107-1
D106-A
R106-1
U1-6
)
(
NET22
D107-K
D106-K
)
(
NET23
R114-1
R113A-1
R113C-1
R113B-1
U1-13
)
(
NET24
R114-2
U1-14
R311-1
)
(
NET25
R108-1
R113B-2
U1-8
)
(
NET26
R108-2
R109-2
U1-9
)
(
NET27
R110G-1
R110-2
U1-10
)
(
NET28
R102B-2
R102C-2
R101-1
R102A-2
U1-2
)
(
NET29
R113A-2
U4-7
U4-12
)
(
NET30
R313-2
U3-13
R313G-1
C313-1
)
(
NET31 (vo/50)
R102C-1
U2-1
U2-2
)
(
NET32 (iL/10)
R110-1
U3-12
U2-8
U2-9
)
(
NET33
C203-2
R203-2
U2-3
)
(
NET34
C210-2
R210-2
U2-10
)
(
NET35
C212-2
R212-2
U2-12
)
(
NET36
C205-1
R205-2
U2-5
)
(
NET37
R024J-1
J25-24
)
(
NET38
R203-1
J25-9
)
(
NET39
R205-1
J25-8
)
(
NET40
R210-1
J25-6
)
(
NET41
R212-1
J25-7
)
(
NET42
U3-1
R301-2
C301-2
D301-K
)
(
NET43
U3-2
U3-8
U3-10
C302-2
)
(
NET44
U3-4
J25-13
)
(
NET45
U3-9
U3-11
R311-2
C311-2
D311-K
)
(
NET46
U3-16
R316B-1
R316A-1
C317-1
D317-K
)
(
NET47
U3-17
U7-3
C317-2
D317-A
)
(
NET48
U3-18
R318-1
)
(
NET49
U7-2
R704-2
R702-2
C702-2
)
(

NET50
U7-7
U5-4
R504-1
)
(
NET51
U8-2
U5-11
)
(
NET52 (vin/50)
U2-6
U2-7
U4-1
)
(
NET53
U5-1
J25-3
R501-1
C501-1
)
(
NET54
U5-2
J25-2
R502-2
)
(
NET55
U5-3
U5-13
J25-1
)
(
NET56
U5-5
J25-14
R505-2
)
(
NET57
U5-6
U5-12
J25-15
)
(
NET58
U5-9
U5-10
R509-1
)
(
NET59
D901A-A
D902A-K
)
(
NET60
D901B-A
D902B-K
)
(
NET61
R907-1
D907-2
)

Netlist for the Phase-Locked Loop Circuit
Filename: PLL.DOC

```
C202
RAD0.2

C102
RAD0.2

R202
AXIAL0.4

R102
AXIAL0.4

R107
AXIAL0.4

R207
AXIAL0.4

C103
RAD0.2

C203
RAD0.2

C204
RAD0.2

C104
RAD0.2

C108
RAD0.3

C308
RAD0.3

C208
RAD0.3

JUMPER
RAD0.2

R311X
AXIAL0.4

R311
AXIAL0.4

T-15
RAD0.2
T+15

RAD0.2

TI_SET
RAD0.2

TSLAVE
RAD0.2

TMASTER
RAD0.2

U2-LM311
DIP8

U1-LM311
DIP8

U3-4011
DIP14

R103
AXIAL0.4

R203
AXIAL0.4

R108
AXIAL0.4

C311
RAD0.2

R208
AXIAL0.4

(
NET1
C202-1
R202-2
U2-LM311-2
)
(
NET2
C102-1
R102-2
U1-LM311-2
)
(
NET3
R202-1
TSLAVE-2
)
(
NET4
R102-1
TMASTER-2
)
(
NET5
R107-1
R207-1
C108-2
C314-2
C208-2
T+15-2
U2-LM311-8
U1-LM311-8
U3-4011-14
R108-2
R208-1
)
(
NET6
R107-2
U1-LM311-7
U3-4011-13
)
(
NET7
R207-2
U2-LM311-7
U3-4011-8
)

(

NET8
C103-1
U1-LM311-3
R103-2
R108-1
)
(
NET9
C203-1
U2-LM311-3
R203-2
R208-2
)
(
NET10
C204-2
C104-2
T-15-1
U2-LM311-4
U1-LM311-4
)
(
NET11
JUMPER-2
U3-4011-10
)
(
NET12
JUMPER-1
U3-4011-12
)
(
NET13
R311X-1
TI_SET-1
)
(
NET14
R311X-2
R311-1
C311-1
)
(
NET15
R311-2
U3-4011-9
U3-4011-11
)
```

Netlist for the IGBT Driver Circuit
Filename: DRIVER.DOC

COMPONENTS

C104,C108
2200uF-50V
RB.3/.6

C148
0.22uF
RAD0.3

C203
0.1uF
RAD0.2

D108A,D104A,
D108B,D104B
1N4005
DIODE0.4

D123
1N4148 or 1N914
DIODE0.4

DGATE2,DGATE1
1N4744-Zener
DIODE0.4

JUMP
-jumper with opto
-input if no opto
RAD0.1

COMPONENTS

R106
6.2-1/4W
AXIAL0.4

R107
1k-1/4W
AXIAL0.4

R201
-jumper with opto
-1.3k-1/4W if no opto
AXIAL0.4

R213
1k-1/4W
AXIAL0.4

U1
TLP250 (Toshiba)
DIP8

U2
HFBR-2521 (HP)
HFBR 15/25XX

VR1
LM78L05ACZ
TO-92A

NETLIST

NET1
JUMP-1
U1-3
D123-A

NET2
R213-1
U2-3
VR1-2
C203-1

NET3
R213-2
U2-4
U2-1
R201-2

NET4
C148-2
C104-2
D104A-A
D104B-A
U1-5

NET5
C148-1
C108-1
D108A-K
D108B-K
U1-8
VR1-1

NET6
D108A-A
D104A-K

NETLIST

NET7
D108B-A
D104B-K

NET8
U1-7
U1-6
R106-2

NET9
U1-2
R201-1
D123-K

NET10
R106-1
DGATE2-A
R107-2

NET11
DGATE2-K
DGATE1-K

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